Course Description

This is a new seminar course which will explore advanced topics in two broad areas that will have a significant influence in computer systems design over the next decade: power related issues (energy/temperature) and reliability. The main learning vehicles will be readings of classic and recent research papers on both topics, followed by in-class discussions and critiques. Students will be expected to participate in all in-class sessions and occasionally lead a discussion. In addition, students will be required to write short (less than a page) critical analyses of the research papers.

This course is geared to graduate students in computer engineering and systems (architecture, VLSI/CAD, embedded systems, operating systems, programming languages/compiler design). There is no formal list of prerequisites, but students are expected to have a basic understanding of computer architecture principles.

Instructor

Professor Russ Joseph
Office: Tech L467
Email: rjoseph@ece.northwestern.edu
Phone: 1-3061
Office Hours: Tuesday and Thursday 3:30pm-5:00pm or by appointment

Class Meetings

Discussion: Tuesday and Thursday 2:00-3:20pm
Discussion: Tuesday 3:00-3:50pm
Location: Tech LG62
Prerequisite
Undergraduate knowledge of computer architecture.

Webpage
The course webpage is available via Blackboard at: http://www.ece.northwestern.edu/rjoseph/ece510-2

Required Textbook
None.

Tentative List of Papers/Topics

Modeling Power in Processors


Managing Dynamic Power


Managing Static Power


**Thermal Considerations**


**Dealing With Power Variations**


**Run-time Monitoring**


**Multiple Clock Domains**
• Power and performance evaluation of globally asynchronous locally synchronous processors

• G. Semeraro, G. Magklis, R. Balasubramonian, D.H. Albonesi, S. Dwarkadas, and M.L. Scott,
  "Energy Efficient Processor Design Using Multiple Clock Domains with Dynamic Voltage and

• Q. Wu, P. Juang, M. Martonosi, and D.W. Clark, "Formal Online Methods for Voltage/Frequency
  Control in Multiple Clock Domain Microprocessors. ASPLOS 2004".

Circuit-Level Timing Speculation

• Dan Ernst, Nam Sung Kim, Shidhartha Das, Sanjay Pant, Toan Pham, Rajeev Rao, Conrad
  Ziesler, David Blaauw, Todd Austin, Trevor Mudge, and Krisztin Flautner, Razor: A Low-
  Power Pipeline Based on Circuit-Level Timing Speculation, in the 36th Annual International
  Symposium on Microarchitecture (MICRO-36), December 2003

Power Aware Chip Multiprocessors

• Single-ISA Heterogeneous Multi-Core Architectures: The Potential for Processor Power Re-
  duction, Rakesh Kumar, Keith Farkas, Norm P. Jouppi, Partha Ranganathan, Dean M.

• Heat-and-run: Leveraging SMT and CMP to manage power density through the operating
  system. Michael Powell, Mohamed Gomaa, and T. N. Vijaykumar In Proceedings of the 11th
  International Conference on architectural support for programming languages and operating
  systems (ASPLOS), pages 260-270, October 2004

Transient Fault Detection and Recovery in SMT/CMP

• Transient-Fault Recovery for Chip Multiprocessors Mohamed Gomaa, Chad Scarbrough, T.
  N. Vijaykumar, and Irith Pomeranz In Proceedings of the 30th Annual International Symposi-

• Opportunistic Transient-Fault Detection Mohamed Gomaa and T. N. Vijaykumar In Pro-
  ceedings of the 32nd Annual International Symposium on Computer Architecture (ISCA),
  pages 172-183, June 2005.

• Transient-Fault Recovery via Simultaneous Multithreading T. N. Vijaykumar, Irith Pomer-
  anz, and Karl Cheng In Proceedings of the 29th Annual International Symposium on Com-
Testability


On-line Hard Error Detection and Tolerance


Architectural Vulnerability

- Shubhendu S. Mukherjee, Christopher Weaver, Joel Emer, Steven K. Reinhardt, and Todd Austin, A Systematic Methodology to Compute the Architectural Vulnerability Factors for a High-Performance Microprocessor, in the 36th Annual International Symposium on Microarchitecture (MICRO-36), December 2003.

- Nicholas J. Wang, Justin Quek, Todd M. Rafacz, and Sanjay J. Patel, Characterizing the Effects of Transient Faults on a High-Performance Processor Pipeline, Proceedings of the 2004 International Conference on Dependable Systems and Networks, Florence, Italy, June 2004

Lifetime Management


Reliability Under Shared Memory


Nano And Emerging Technologies


Clumsy Processors


Discussion and Reading Assignments

The primary learning vehicles in this course will be the reading of technical papers and participation in class discussions. Nominally, the instructor will assign readings a week in advance (typically two papers per class meeting). Students are expected to have read the papers carefully and constructed a critical analysis of each paper.

The critical analysis should clearly identify strengths/contributions of the paper as well as potential weaknesses and areas for further work. In addition, students are encouraged to compare and contrast the approach/findings with other relevant work. Each critical analysis should be emailed to the instructor (plain text or ps/pdf are preferable) by class time the day the paper is to be discussed.

Everyone benefits from a lively discussion, so be prepared for in class discussion by doing your reading!

Occasionally (about twice during the quarter), each student will lead discussion on a research paper. Students should be prepared to give a brief summary of the work (using visual aids, e.g. PowerPoint or the blackboard when appropriate). Choice of topics/papers is on a first come-first serve basis. If you see a paper/topic that interests you, ask the instructor if you can lead the corresponding discussion. Schedule early to improve your chances of getting your first pick.

Pariticpation and Attendance

The quality of this course depends heavily on preparation, attendance, and participation of all the students. To that end, a significant component of the grade for this class will be your perfor-
mance/participation in class discussions. If you are unable to attend a class meeting, please email the instructor before hand.

Exams

There will be no exams in this class.

Grading

Grades will be assigned according to the following distribution:

- Participation  50%
- Critical Analysis  25%
- Leading Discussion  25%

Because the grading in this class is more subjective than most technical classes, the instructor will give frequent feedback, so that students can make suitable adjustments.