Sample Final Examination

There are six questions. Be precise, show every step, and state your assumptions (if any), to get full credit.

1. (20 pts) Given a four-input Boolean function, \( f(A, B, C, D) = \sum m(0, 3, 5, 7, 11, 12, 13, 15) \)
   (a) Implement the function using a 16:1 multiplexer.
   (b) Implement using an 8:1 multiplexer.
   (c) Implement using a 4:1 multiplexer.
   (d) Implement the function using a 4:16 decoder and an OR gate.

2. (10 pts) Make the following two-level logic designs hazard free under one input switching:
   (a) \( F(A, B, C, D) = \sum m(0, 1, 2, 5, 8, 9, 10, 13) \)
   (b) \( G(A, B, C, D) = (A + C)(\bar{A} + D)(\bar{B} + \bar{C} + D) \)

3. (10 pts) Design a positive edge-triggered T flip-flop by using only NAND gates.

4. (20 pts) Minimize the state diagram in Figure Ex9.5 on Katz page 489. Then make a state assignment and implement it by using D flip-flops.

5. (20 pts) Model the given designs in VHDL language.

6. (20 pts) A sequential circuit has two inputs and two outputs. The inputs \((X_1, X_2)\) represent a 2-bit binary number, \(N\). If the present value of \(N\) is greater than the previous value, then \(Z_1 = 1\). If the present value of \(N\) is less than the previous value, then \(Z_2 = 1\). Otherwise, \(Z_1\) and \(Z_2\) are 0.
   (a) Derive a Mealy machine state diagram and make sure it is minimized.
   (b) Derive a Moore machine state diagram and make sure it is minimized.