Design and Implementation a Finite Impulse Response (FIR) Filter

The FIR filter is widely used in various DSP applications such as signal preconditioning, video convolution functions, and communications. Figure 1 is an example of the architecture of an 8-tap FIR filter. The input is shifted through 8 registers (taps). Each output stage of a particular register is multiplied by a known coefficient. The resulting outputs of the multipliers are then summed to create the filter output.

![Figure 1: FIR Filter Traditional Architecture, 8 Tap.](image)

Design an 8-tap FIR filter and implement targeting the Xilinx Spartan-2 xc2s50 FPGA in Xilinx ISE environment. Demonstrate the correct operation by simulation results. The clock frequency of your design should be at least 120 MHz.

There are some resources posted for reference. Note that there are various different ways of implementing this circuit, hence, there will be multiple correct solutions. Create your most optimal fastest original solution. Consider the decisions you need to make to trade-off resources (parallelism) vs. speed. Use 8-bit fixed point arithmetic. Use the following coefficients: \(c_1 - c_7 = [1 2 3 4 5 6 7 8]\). Pick an arbitrary input sequence.

Your report should include
- Descriptive block level diagram of your design
- Detailed explanation of your design decisions and experience
- Simulation Results verifying correct operation
- (In conjunction with the item above) Demonstration that the filter is able to smooth out noise in a given input sequence.
- Implementation results presenting the area and delay of your circuit.

**Bonus (10 Points):** Compare the output of your filter against a Matlab simulation of the same filter.