Gate Sizing for Crosstalk Reduction under Timing Constraints by Lagrangian Relaxation

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Outline

• Introduction
• Modeling
• Problem formulation
• Gate sizing by Lagrangian Relaxation
• Experimental results
• Conclusions
Introduction

• Crosstalk / Coupling noise – Functionality failure
• Coupling induced delay variations – Timing violation

* from Technology white paper – Sequence Design Inc.
Prior work: Gate sizing for crosstalk reduction

- Post route
  - Scalable libraries
  - Existing fill space
- Shown effective
  - Xiao et al. [ASP DAC 99]
  - Hashimoto et al. [ISPD 02]
  - Becer et al. [DAC 03]
  - Sinha et al. [ISPD 04]
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• **Modeling**
• Problem formulation
• Gate sizing by Lagrangian Relaxation
• Experimental results
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Modeling

\[ c_5(s_5) \]

\[ r_4(s_4) \]

\[ C_x \]

\[ R_w \]

\[ C_w / 2 \]

Coupling graph

Required arrival time \( \leq A_0 \)

(Timing Constraint)

\[ N_i \leq U_i \]

(Noise Constraint)
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Gate sizing problem

- Minimize weighted sum of gate-sizes under given constraints
  - Area optimization
  - Power optimization

\[
\text{Minimize } \sum_{i=0}^{n-1} w_i \cdot s(i)
\]

such that –

- Timing constraint
  \[ T_{\text{arrival}}(PO) \leq A_0 \]
- Noise constraints
  \[ N(i) \leq U(i) \quad \forall i \in \text{nets} \]
- Size constraints
  \[ l(i) \leq s(i) \leq u(i) \quad \forall i \in \text{gates} \]
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Gate sizing problems

- Determine optimal gate sizes under constraints for timing and crosstalk reduction

\[
\text{Minimize } \sum_{i=0}^{n-1} w_i \cdot s(i)
\]

such that –

- \( \overline{T_{\text{arrival}}(PO)} \leq A_0 \)
- \( N(i) \leq U(i) \quad \forall i \in \text{nets} \)
- \( l(i) \leq s(i) \leq u(i) \quad \forall i \in \text{gates} \)

- Optimal gate sizing for coupling & wire sizing by iterative fixpoint computation using Lagrangian relaxation - Chen et al. [TCAD 99]
- Optimal gate sizing for coupling-noise reduction by iterative fixpoint computation - Sinha et al. [ISPD 04]
Lagrangian Relaxation (LR)

• Simplify the optimization problem
  • Relax “troublesome” constraints
  • Incorporate them into the objective function

• LR Sub-problem (LRS)
  \[ Z = \max \ f(x) \quad \text{such that} \quad g(x) \leq A, \ h(x) \leq B \]
  \[ Z(u) = \max \ f(x) + (A - g(x))u \quad \text{such that} \quad h(x) \leq B \]

• Lagrangian Dual Problem (LDP)
  • Optimal \( u^* \) : Solution to LRS same as original problem
  • Sub gradient optimization
Gate sizing for timing

[ Chen et al. – TCAD 99 ]

Optimize gate sizes under timing constraints

\[ \text{Minimize } \sum_{i=0}^{n-1} w_i \cdot s(i) \]

such that –

- \( a_j \leq A_0 \quad \forall j \in \text{input}(PO) \)
- \( a_j + D_i \leq a_i \quad \forall i \cap j \in \text{input}(i) \)
- \( l(i) \leq s(i) \leq u(i) \quad \forall i \in \text{gates} \)

Timing constraint
Gate sizing for crosstalk reduction

Optimize gate sizes under noise constraints

\[
\text{Minimize } \sum_{i=0}^{n-1} w_i \cdot s(i)
\]

such that –

\[
N(i) \leq U(i) \quad \forall i \in \text{nets}
\]

\[
l(i) \leq s(i) \leq u(i) \quad \forall i \in \text{gates}
\]
Monotonicity of the noise function

• **Sizing up driving gate of a net**
  - Decreases induced noise on itself
  - May increases noise on coupled nets

• **Vice versa**

Net N1 (Victim): Affected by coupling noise from nets N2 and N3

- Sizing up driving gate of N1 reduces noise on itself, but it acts as an aggressor now!
- Driving gate of N2 sized down to reduce noise on N1. It now becomes a victim!
Gate sizing for crosstalk reduction
[ Sinha et al. – ISPD 04 ]

- Developed a gate sizing transformation
  - $g_i = \min (\text{driving gate size of net } i) : \text{No noise violation on net } i$, given driving gate sizes of coupled nets
  - Monotonic transformation guarantees optimality when starting from minimum gate-sizes
  - Optimal solution is a fixpoint of the transformation
Need for combined optimization

• Multi-stage optimization
  ▪ Timing $\rightarrow$ Crosstalk
    • Circuit may violate timing constraint
  ▪ Crosstalk $\rightarrow$ Timing
    • New noise violations may be introduced

• Combined optimization
  ▪ Timing + Crosstalk
    • Handle constraints simultaneously
Gate sizing problem

Optimize weighted sum of gate sizes under constraints

$$\text{Minimize } \sum_{i=0}^{n-1} w_i \cdot s(i)$$

such that –

- $a_j \leq A_0$ $\forall j \in \text{input(PO)}$
- $a_j + D_i \leq a_i$ $\forall i \cap j \in \text{input}(i)$
- $l(i) \leq s(i) \leq u(i)$ $\forall i \in \text{gates}$
- $N(i) \leq U(i)$ $\forall i \in \text{nets}$

Timing constraints

Noise constraints
Gate sizing by Lagrangian Relaxation

- Relax constraints on arrival times
  - Sub-problem objective a posynomial
  - Leverage fixpoint computation approach

\[
\begin{align*}
\text{Minimize} & \quad \sum_{i=0}^{n-1} w_i s(i) + \sum_{j \in \text{input}(PO)} \lambda_{j0} (a_j - A_0) \\
& + \sum_{i=0}^{n-1} \sum_{j \in \text{input}(i)} \lambda_{ji} (a_j + D_i - a_i) \\
\text{such that} & \quad N(i) \leq U(i) \quad \forall i \in \text{nets} \\
& \quad l(i) \leq s(i) \leq u(i) \quad \forall i \in \text{gates}
\end{align*}
\]

Lagrange multipliers
Simplifying the LRS

• Reformulate problem as

\[ \text{Minimize } \sum_{i=0}^{n-1} w_i s(i) + \sum_{i=0}^{n-1} \mu_i D_i \]

\[ \text{such that } \]

\[ \mu_i = \sum_{j \in \text{input}(i)} \lambda_{ji} \]

\[ N(i) \leq U(i) \quad \forall i \in \text{nets} \]

\[ l(i) \leq s(i) \leq u(i) \quad \forall i \in \text{gates} \]
Solving the Lagrangian sub-problem – LRS(µ)

\[ L_\mu(S) = \sum_{i=0}^{n-1} w_i s(i) + \sum_{i=0}^{n-1} \mu_i D_i = A_i(S) \cdot s(i) + \frac{B_i(S)}{s(i)} + E_i(S) \]

Define local refinement functions

\[ h_i(S) = \min \{ s(i) : L_\mu \} = \sqrt{\frac{B_i(S)}{A_i(S)}} \]

Function of upstream resistance, downstream capacitance ...

Noise constraint satisfied on all driven nets

\[ g_i(S) = \min \{ s(i) : N(i) \leq U(i) \} \]
Solving the Lagrangian sub-problem – LRS(μ)

\[ L_\mu(S) = \sum_{i=0}^{n-1} w_i s(i) + \sum_{i=0}^{n-1} \mu_i D_i = A_i(S) \cdot s(i) + \frac{B_i(S)}{s(i)} + E_i(S) \]

L_\mu is convex

\[ \phi_i(S) = \min[u(i), \max(l(i), g_i(S), h_i(S))] \]
Algorithm : Solve LRS(µ)

• begin
  ▪ init driver sizes to minimum : \( s(i) = l(i), \; \forall i \in (0, n-1) \)
  ▪ do for each gate
    • evaluate \( g_i(S) \)
    • evaluate \( h_i(S) \)
    • \( s(i) = \phi_i(S) \)
  ▪ while (no further improvement)
• return gate-sizes
• end
Solving the Lagrangian Dual Problem – LDP

- Sub gradient optimization
  - Start with arbitrary non-negative $\lambda_{ij}$’s
  - Move to new point
    - Multiply sub-gradient direction by step size $\rho_k$
    - Add to $\lambda$ – Ensure conditions are satisfied
      \[
      \lambda_{ji} = \begin{cases} 
      \lambda_{ji} + \rho_k (a_j - A_0) & \text{if } i = PO \\
      \lambda_{ji} + \rho_k (a_j + D_i - a_j) & \text{otherwise}
      \end{cases}
      \]
  - Repeat till convergence
    - Can be guaranteed under conditions on $\rho_k$
Crosstalk aware gate sizing algorithm

- Input: Layout extraction results
- begin
  - construct DAG from circuit
  - superimpose coupling-graph
  - call $LDP \rightarrow$ optimal Lagrange multipliers $\mu$
  - call $LRS(\mu)$
- end
Optimality guaranteed in special cases

- Optimal solutions to sizing problems
  - $S^*$ $\rightarrow$ timing
  - $S^{**}$ $\rightarrow$ timing + noise
- If $S^*$ and $S^{**}$ have an ordering

Given by monotonic properties of $h(S)$ and $\phi(S)$

Proposed heuristic yields optimal solution = $S^{**}$
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Experimental setup

• ISCAS’85 benchmarks and larger circuits
  ▪ 200 – 20,000 nodes (Runtime < 75 secs)
  ▪ Parameters – 0.18µ technology
• 2Π model – crosstalk modeling (Cong et al.)

Comparisons

• Proposed approach
  ▪ Timing + Noise
• Multi-stage approach
  ▪ Timing – Circuit optimized using LR for timing [Chen et al. TCAD99]
  ▪ Timing → Noise – Further noise optimization [Sinha et al. ISPD 04]
## Noise reduction results – I

<table>
<thead>
<tr>
<th>Circuit</th>
<th># Node</th>
<th># CEdge</th>
<th>Timing</th>
<th>Timing → Noise</th>
<th>Timing + Noise</th>
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</tbody>
</table>

- **Area Gain = 1.5%**
- **All violations removed**
- **Area Gain = −4.3%**

- **$U_i = 0.2V_{dd}$**
- **Required time = 1.0**
### Noise reduction results – II

- $U_i = 0.1V_{dd}$
- Required time $= 1.0$

<table>
<thead>
<tr>
<th>Circuit</th>
<th># Node</th>
<th># CEdge</th>
<th>Timing</th>
<th>Timing $\rightarrow$ Noise</th>
<th>Timing $+$ Noise</th>
</tr>
</thead>
<tbody>
<tr>
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</tr>
</tbody>
</table>

- Area Gain = 5.4%
- NV Gain = 12
- Area Gain = 18.4%
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Conclusions

• Gate sizing for crosstalk reduction
  • Timing constrained
  • Based on Lagrangian Relaxation
• Shown effective
  • Comparisons to design methodology of independent sizing for timing and crosstalk successively

Thank You