Arindam Mallik

Mobile: 0032-485978802
arindam@imec.be
http://www.arindam.net

Kapeldreef 75
B-3001, Leuven,
Belgium

OBJECTIVE

Research scientist pursuing a research and development position in the field of system design and architecture.

RESEARCH INTERESTS

Embedded Systems, MPSoC architecture, Memory modeling, Power & Performance Analysis, System Design and Verification, Reliability, User-aware system design, Network Processors, Low Power Design, Microarchitecture

QUALIFICATION OVERVIEW

- Well-qualified and technically-proficient Research Scientist with more than eight years research experience and excellent academic qualifications.
- Substantial experience in sophisticated research techniques and technologies: power-performance trade-off analysis, dynamic voltage and frequency management, role of users in mobile computing.
- Organized, take-charge professional with exceptional follow through abilities and detail orientation, able to plan and oversee projects from concept to successful conclusion.
- Expertise in lab and field research, data collection/analysis and project management.
- Extensive experience working with cross-functional collaborative scientific and research teams.

ACADEMIC BACKGROUND

- *PhD in Computer Engineering,* 2004 – 2008
  Dissertation- "Holistic Computer Architectures based on Application, User, and Process Characteristics"
  Department of Electrical Engineering & Computer Science, Northwestern University, USA
- *MS in Computer Engineering,* 2002 – 2004
  Thesis- "Low Power Algorithm for Optimization with Quantization Error Constraints in SystemC based ASIC Design"
  Department of Electrical & Computer Engineering, Northwestern University, USA
- *Bachelor of Computer Sc. & Engineering (First Class with honors)* 1998 – 2002
  Department of Computer Science & Engineering, Jadavpur University, India

INDUSTRY EXPERIENCE

IMEC vzw, Smart Systems and Energy Technology (Leuven, Belgium) March, 2009- Present
Specialist Researcher

- Project coordinator for 3M Euro EU funded MPSoC Memory Optimization project.
- Managing overall collaboration between 4 European universities and 2 European Company.
- Involved in the development of a system-level model for emerging memory technology
- Developing a middleware tool to trade-off system level parameters based on technology parameters

IMEC vzw, Smart Systems and Energy Technology (Leuven, Belgium) September, 2008 – February, 2009
Researcher

- Technical leader from IMEC for the EU funded MPSoC Memory Optimization project.
- Worked on Memory architecture of MPSoC sysems.
- Involved in the development of a source-to-source optimization framework for multicore embedded systems
- Built an integrated framework for combining design-time and runtime techniques to improve cost-efficiency and performance of multicore embedded systems platform.

Intel Corporation, Systems Technology Lab (Hillsboro, OR, USA) June-December, 2006
Research Intern

- Worked on many-core processor platform power modeling.
- Designed a dynamic power model for the memory subsystem.
- Proposed user-aware power management scheme for many-core ultra mobile devices.

Cswitch Corporation (Santa Clara, CA, USA) June-September, 2005
Research Intern
- Involved in the design of a datapath for a reconfigurable network processor.
- Analysis of Benchmark applications in different reconfigurable logic family.

Atrenta Inc. (Noida, India) June-September, 2003
Summer Intern
- Development of a Verilog compiler for the SpyGlass Predictive Analyzer software.
- Compatibility issues and benchmarking in Verilog-2001.

RESEARCH DETAILS

Current Research
Smart Systems & Technology, IMEC, Belgium

Source-to-source optimizations of statically allocated data mapping on MPSoC platforms [C1, C2, C3]
- Performed Power-Performance tradeoff analysis for Scratchpad memory architecture.
- Introduced automatic parallelization of serialized application in embedded systems domain.
- Integrated tools to result an automatic framework for parallelizing embedded applications optimally in MPSoC

Doctoral Research
Dept. of EECS, Northwestern University, USA
Research Advisor: Prof. Gokhan Memik

Correctness Trade-Offs in Application Specific Processors [J3, C15, C17]
- Performed Reliability-Performance Tradeoff analysis for Level-1data cache for packet processors.
- Introduced a realistic analytical model to determine the probability of a fault in a cache.
- Introduction of a new generic parameter for reliability and performance tradeoff in processors.
- Adaptive architecture to improve performance/energy consumption of application specific processors.

Variable Latency Cache [C9]
- Developed a non-uniform access Level-1 data-cache based on variability in access latency.
- Analyzed the impact of coupling and physical location on cache access latencies.

User-Aware Power Management [J5, C6, C7, C10, C11, T1, T3, P1, P2]
- Dynamic Voltage and Frequency Scaling in a mobile processor based on user behavior.
- Measurement of user-perceived performance and using it for DVFS.
- Prediction of user behavior based on their response to the DVFS of the system.
- Analysis of user annoyance in response to system power management.

Task Allocation in Multicore Processors Using Statistical Variation [C8]
- Utilizes statistical information to process network packets in multi-core processors.
- Efficient task scheduling algorithm based on statistical properties of networking applications.
- Improved scalability and utilization of processing cores in a multi-core environment.

Process and Thermal-Aware Voltage Setting [J4, C10, C11, T1]
- Explored the effect of process variation on the supply voltage of a processor.
- Proposed a Dynamic Voltage Setting schema customized for individual processor and operating temperature.

Low Power Caches for Network Processors
- Introduction of a new cache architecture for improved performance and reduced energy consumption in Network Processors (NPU)

Masters Research
Dept. of EECS, Northwestern University, USA
Research Advisor: Prof. Prith Banerjee

Power Aware Architectural and Compilation Techniques Project [J4, C12]
- Area and Power Optimization with error constraints during high level synthesis of ASIC Design.
- A new methodology for precision analysis through the combined use of simulation, high level synthesis, user input, and program analysis.

JOURNAL PUBLICATIONS:

J1. Jack Cosgrove, Arindam Mallik, Gokhan Memik, Robert P. Dick, Peter Dinda, "*PICSEL: Measuring User-Perceived Performance to Control Dynamic Voltage and Frequency Scaling*", *submitted* to ACM Transactions on Architecture and Code Optimization (ACM-TACO)

J2. Song Liu, Arindam Mallik, Seda O. Memik, "*An Instruction-Based Switching Model for Dynamic Power Management*", *submitted* to ACM Transactions on Design Automation of Electronic Systems (ACM-TODAES)

J3. Arindam Mallik, Gokhan Memik, "*Analyzing Correctness-Perforamce Trade-offs: Clumsy Packet Processors*", *submitted* to ACM Transactions on Architecture and Code Optimization (ACM-TACO)

J4. Arindam Mallik, Debjit Sinha, Prith Banerjee, and Hai Zhou, "*Low Power Optimization by Smart Bit-width Allocation in a SystemC based ASIC Design Environment*", IEEE Transactions on Computer-aided Design of Integrated Circuits and System (IEEE-TCAD), Volume 26, Number 3, March 2007

J5. Arindam Mallik, Bin Lin, Gokhan Memik, Peter Dinda, Robert P. Dick, "*User-Driven Frequency Scaling*", IEEE Computer Architecture Letters (IEEE-CAL), Volume 5, no. 2, 2006

J6. Arindam Mallik and Gokhan Memik "Low *Power Correlating Caches for Network Processors*", Published in The Journal for Low Power Electronics (JOLPE). Volume 1, Number 2, August 2005

J7. Arindam Mallik, M. Wildrick and Gokhan Memik, "*Application-Level Error Measurements for Network Processors*", In Institute of Electronics, Information and Communication Engineers Transactions on Information and Systems (IEICE-TIS), Volume E88-D, Number 8, August 2005

CONFERENCE PUBLICATIONS:

C1. Yannis Iosifidis, Arindam Mallik, Stylianos Mamagkakis, Eddie De Greef, Alexis Bartzas, Dimitros Soudris, Francky Catthoor, *"A Framework for Automatic Parallelization, Static and Dynamic Memory Optimization in MPSoC Platforms"*, in the Design Automation Conference (DAC-2010), Anaheim, CA, June 2010

C2. Arindam Mallik, Maryse Wouters, Peter Lemmens, Eddy De Greef, Tomas Ashby, *"Source-to-source optimizations of statically allocated data mapping on MPSoC platforms"*, in the DATE Workshop on Designing for Embedded Parallel Computing Platforms: Architectures, Design Tools, and Applications (DATE-2009), April 2009

C3. Arindam Mallik, Maryse Wouters, Peter Lemmens, Christos Baloukas, Robert Pyka, Dimitros Kritharidis, Francois Capman, and Sander Stuijk, *"MNEMEE: Memory management technology for adaptive and efficient design of embedded systems"*, in the DATE Workshop on Designing for Embedded Parallel Computing Platforms: Architectures, Design Tools, and Applications (DATE-2009), April 2009

C4. Bin Lin, Arindam Mallik, Peter Dinda, Gokhan Memik, Robert Dick, *"User- and Process-Driven Dynamic Voltage and Frequency Scaling"*, in International Symposium on Performance Analysis of Systems and Software (ISPASS), Boston, MA, April 2009

C5. Alex Shye, Berkin Ozisikyilmaz, Arindam Mallik, Gokhan Memik, Peter Dinda, Robert Dick, Alok Choudhary, "*Learning and Leveraging the Relationship between Architecture-Level Measurements and Individual User Satisfaction Scaling*", *in* The 35th International Symposium on Computer Architecture (ISCA-2008)

C6. Alex Shye, Lei Yang, Xi Chen, Berkin Ozisikyilmaz, Arindam Mallik, Bin Lin, Gokhan Memik, Peter A. Dinda, and Robert P. Dick, *"Empathic Computer Architectures and Systems"*, *in* the International Conference on Architectural Support for Programming Languages and Operating Systems: Wild and Crazy Ideas Session (ASPLOS WACI)

C7. Arindam Mallik, Jack Cosgrove, Gokhan Memik, Robert P. Dick, Peter Dinda, "*PICSEL: Measuring User-Perceived Performance to Control Dynamic Frequency Scaling*", *in* The International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS-2008)

C8. Arindam Mallik and Gokhan Memik, "*Automated Task Distribution in Multicore Network Processors using Statistical Analysis*", *in* The Symposium on Architectures for Networking and Communications Systems (ANCS-2007)

C9. Serkan Ozdemir, Arindam Mallik, Gokhan Memik, "*Variable Latency Caches using Access Time Prediction for Nanoscale Processors*", *in* the International Conference for High Performance Computing, Networking, Storage and Analysis (SC-2007), (*Winner of the best student paper award*)

C10. Peter Dinda, Gokhan Memik, Robert P. Dick, Bin Lin, Arindam Mallik, Asish Gupta, and Samuel Rossoff, *"The User in Experimental Computer Systems Research"*, in the Workshop on Experimental Computer Science in conjunction with The Federated Computer Research Conference (FCRC-2007), June 2007, California, USA

C11. Bin Lin, Arindam Mallik, Gokhan Memik, Peter Dinda, Robert P. Dick, "*Power Reduction Through Measurement and Modeling of Users and CPUs*", in the Proc. of International Conference on Measurement and Modeling of Computer Systems (ACM SIGMETRICS-2007), June 2007, California, USA

C12. Arindam Mallik, Debjit Sinha, Prith Banerjee, Hai Zhou, "*Smart Bit-width Allocation for Low Power Optimization in a SystemC based ASIC design Environment*", in the Proc. of Design, Automation and Test in Europe (DATE-2006), March 2006, Munich, Germany

C13. Gokhan Memik, Masud H. Chowdhury, Arindam Mallik, Yehea I. Ismail, "*Engineering Over-Clocking: Reliability-Performance Trade-Offs for High-Performance Register Files*", in the Proc. of International Conference on Dependable Systems and Network (DSN-2005), June, 2005, Yokohama, Japan

C14. Gokhan Memik, Mahmut T. Kandemir, Arindam Mallik, "*Load Elimination for Low-Power Embedded Processors*", in the Proc. of Great Lakes Symposium on VLSI 2005 (GLSVLSI-2005), April 2005, Chicago, IL

C15. Arindam Mallik and Gokhan Memik, "*A Case for Clumsy Packet Processors*", in the Proc. of International Symposium on Microarchitecture (MICRO-2004), December 2004, Portland, OR

C16. Arindam Mallik and Gokhan Memik, "*Design and Study of Correlation Cache*", in the Proc. of International Symposium on Low Power Electronic Design (ISLPED-2004), August 2004, Newport Beach, CA

C17. Arindam Mallik, Matthew Wildrick, Gokhan Memik, "*Measuring Application Error Rates for Network Processors*", in the Proc. of Intl. Midwest Symposium on Circuits and Systems (MWSCAS-2004), July 2004, Hiroshima, Japan

TECHNICAL REPORT:

T1. Arindam Mallik, "*Holistic Computer Architectures based on Application, User, and Process Characteristics*", PhD Thesis, Northwestern University, March 2008
T2. Arindam Mallik, Jack Cosgrove, Gokhan Memik, Robert P. Dick, Peter Dinda, "*PICSEL: Measuring User-Perceived Performance to Control Dynamic Frequency Scaling*", Technical Report NWU-EECS-06-11, Department of Electrical Engineering and Computer Science, Northwestern University, August, 2007
T3. Serkan Ozdemir, Ja C. Ku, Arindam Mallik, Gokhan Memik,; Yehea Ismail, "*Variable Latency Caches for Nanoscale Processor*", Technical Report NWU-EECS-06-16, Department of Electrical Engineering and Computer Science, Northwestern University, November, 2006
T4. Arindam Mallik, Bin Lin, Peter Dinda, Gokhan Memik, and Robert P. Dick, "*Process and User Driven Dynamic Voltage and Frequency Scaling*", Technical Report NWU-EECS-06-11, Department of Electrical Engineering and Computer Science, Northwestern University, August, 2006
T5. Arindam Mallik, " *An Algorithm for Low Power Optimization with Quantization Error Constraints in SystemC based ASIC Design*", MS Thesis, Northwestern University, March 2004
T6. Arindam Mallik and Jyotirmoy Das, "*Synthesis of Hierarchical Cellular Automata and Application in Authentication*", BE Final Year thesis, Jadavpur University, June 2002

PATENTS:

P1. Arindam Mallik, Bin Lin, Peter Dinda, Gokhan Memik, Robert P. Dick, "*Systems and Methods for Process and User Driven Dynamic Voltage and Frequency Scaling* ", IPC8 Class: AG06F900FI, USPC Class: 7131, 02-05-2009.
P2. Jack Cosgrove, Arindam Mallik, Gokhan Memik, Robert P. Dick, Peter Dinda, "*PICSEL: Measuring User-Perceived Performance to Control Dynamic Voltage and Frequency Scaling*", under Northwestern University Technology Transfer Program, April 2008.

GRANT WRITING EXPERIENCE:

G1. Adjusting Architectures/Circuits for Improved Performance and Reduced Design Complexity 04/2006 – 04/2009
Source: National Science Foundation (NSF)
Amount: $450,000; Investigators: Gokhan Memik (PI), Seda O. Memik, Russ Joseph, Yehea Ismail
G2. High Performance Networking Hardware Design 08/2005 – 08/2008
Source: Department of Energy (DOE)
Amount: $300,000; Investigators: Gokhan Memik (PI)

TEACHING EXPERIENCE:

T1. Teaching Assistant, ECE 202: Introduction to Electrical Engineering, Instructor: T. Pappas, Spring 2005.
T2. Teaching Assistant, ECE 361: Computer Architecture, Instructor: G. Memik, Winter 2004.
T3. Teaching Assistant, ECE 202: Introduction to Electrical Engineering, Instructor: T. Pappas, Fall 2004.
T4. Teaching Assistant, ECE 230: Object Oriented Programming for Engineers, Instructor: Y. Wu, Spring 2004.
T5. Teaching Assistant, ECE 230: Object Oriented Programming for Engineers, Instructor: L. Henschen, Winter 2003.
T6. Teaching Assistant, ECE EA1: Engineering First, Instructor: A. Taflove, Spring 2003.

KEY SKILLS

- Programming Languages: C, C++, Verilog, SystemC, Perl, Javascript, Windows batch scripts,
- Architectural Simulation Framework: Simplescalar Simulator, CACTI, Click modular router, Intel PLATO
- Software Tools: gcc, gdb, Visual Studio, Microsoft .NET, Eclipse, flex, bison
- EDA Tools: Cocentric SystemC Compiler, Synopsys Design Compiler, Mentor Graphics tools

HONORS AND AWARDS:

- Recipient of the best student paper award in the International Conference for High Performance Computing, Networking, Storage and Analysis (SC-2007)
- Recipient of the "*Royal E. Cabell Fellowship*" award on year 2006-07 for terminal year of Doctoral thesis dissertation by The Graduate School, Northwestern University.
- Recipient of the "*Walter P. Murphy Fellowship*" award on year 2002 by the Robert R McCormick School of Engineering and Applied Science, Northwestern University.
- Recipient of the *National Scholarship* from year 1996-2002 under the National Talent Search Scheme, India.

REVIEWER:

- DAC, DATE, ACM-SAC, DSN, EUC, GLSVLSI, ISCA, ISPASS, IISWC

EXTRA CURRICULAR ACTIVITIES:

- Serves as a panel member in the InNUvation, Northwestern University student entrepreneur's panel.
- Executive committee member of Graduates in Electrical Engg. & Computer Sc. (GEECS) at Northwestern University.

AFFILIATIONS:

- Member of IEEE; Member of IEEE Computer Society; Member of ACM

REFERENCES:

- Will be furnished on request