VLSI Design and CAD, 2000–2001

Research Projects

MATCH: A MATLAB Compilation Environment for Adaptive Computing Systems
P. Banerjee* and A. N. Choudhary*
Sponsor: Defense Advanced Research Projects Agency

Adaptive computing systems constitute a new class of computing and communication technology composed of configurable hardware capable of system-level adaptation. Such systems are often built out of combinations of microprocessor-based embedded systems, specialized digital signal processors (DSP's), and field-programmable gate arrays (FPGA's). The objective of this project is to make it easier for users to develop efficient codes for adaptive computing systems. As part of this project, we are developing a compiler that allows input of a user's applications written in the high-level language, MATLAB, and generates efficient low-level code that runs on commercial off-the-shelf FPGA's, embedded processors, and DSP's. Our specific aims include:

- development of a hardware testbed consisting of FPGA's, embedded processors, and DSP's;
- development of a basic compiler for mapping a given MATLAB application onto this heterogeneous target;
- investigation of automated parallelization and mapping techniques;
- design and support of compiler directives;
- development of library functions and applications of interest to DOD;
- development of faster algorithms for compilation.

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*Denotes VLSI Design and CAD faculty member(s), listed in alphabetical order.

PACT: Power-Aware Architectural and Compilation Techniques
P. Banerjee*, A. N. Choudhary*, and H. Yuen
Sponsor: Defense Advanced Research Projects Agency

The objective of the PACT Project is to develop power-aware architectural techniques and associated compiler and CAD tool support. The specific goals of the PACT project are:

- Develop novel architectural and compiler concepts at various levels that can reduce the total energy consumption in specific applications by factors of 10-100X over conventional, non-power-aware architectures.
- Develop compiler techniques to automate the process of generating efficient code that is within a factor of two of the best manual approach with respect to optimizing power under performance and resource constraints.
- Demonstrate the usefulness of the compiler and architectural concepts on some real applications.

We will target specific algorithms / applications that are of interest to DOD. Moreover, we will develop a prototype of a general-purpose memory system chipset to be used on a variety of systems and applications.

PANTHER: A High-Performance Distributed-Computing Infrastructure
P. Banerjee*, A. N. Choudhary*, P. Scheuermann, and V. Taylor
Sponsor: National Science Foundation

Specific aims of this project include:

- Explore using high-speed networking and computing to investigate file-systems and data-management issues for high-performance distributed computing.
- Investigate the parallel-programming support of networks of high-speed workstations and personal computers as an alternative to stand-alone parallel computers.
- Investigate high-performance CAD of electronic systems in a heterogeneous environment.
- Develop a Web-based CAD computing center that takes advantage of high-speed networking.
- Explore new instructional techniques that take advantage of high bandwidth and high speed.

On-Chip Interconnect Noise in Global Distribution Networks
Y. I. Ismail*
Sponsor: Semiconductor Research Corporation / University of Rochester

This project deals with accurately evaluating the responses and signal integrity of global on-chip networks such as clock-distribution and power-distribution networks and buses. As part of the project several tools are being developed for the accurate evaluation of interconnects including inductance effects. Also, design methodologies and interconnect-optimization tools are being developed under this project.

Professional Society Activities

P. Banerjee*, Recipient, Taylor L. Booth Education Award of the IEEE Computer Society, Feb. 2001.

Journals Edited

P. Banerjee*, Assoc. Editor, *IEEE Trans. Computers*.

P. Banerjee*, Assoc. Editor, *IEEE Trans. Parallel and Distributed Systems*.

A. N. Choudhary*, Assoc. Editor, *IEEE Trans. Parallel and Distributed Systems*.

A. N. Choudhary*, Subject Area Editor, *J. Parallel and Distributed Computing*.

Y. I. Ismail*, Assoc. Editor, *IEEE Trans. Very Large Scale Integration (VLSI) Systems*.

Y. I. Ismail*, Assoc. Editor, *IEEE Trans. Circuits and Systems I. Fundamental Theory and Applications*.

Y. I. Ismail*, Guest Editor, *Special Issue IEEE Trans. VLSI Systems on On-Chip Inductance in High-Speed Integrated Circuits*.

Symposia and Symposia Sessions Organized or Chaired

A. N. Choudhary*, Member, Program Committee, HPCA-8.

Y. I. Ismail*, Moderator, panel discussion on "Effects of VLSI Advances on Telecommunication Technologies," at *IEEE Midwest Symp. Circuits and Systems*., Aug. 2000.

Book

Y. I. Ismail* and E. G. Friedman, *On-Chip Inductance in High-Speed Integrated Circuits*, Kluwer, 2001.

Book Sections and Chapters

A. Jones, D. Bagchi, S. Pal, A. Choudhary*, and P. Banerjee*, "PACT HDL: A C-Compiler Targeting ASICs and FPGAs with Power and Performance Optimizations," in *Power-Aware Computing*, R. Melhem and B. Graybill, eds., Kluwer, 2001.

M. Kandemir and A. Choudhary*, "I/O Programming Paradigms: Past and Future," in *High-Performance Mass Storage and Parallel I/O: Theory and Practice*, H. Jin, T. Cortes, and R. Buyya, eds., IEEE Press, 2000.

H. Nagesh, S. Goil, and A. Choudhary*, "Parallel Algorithms for Clustering High-Dimensional Large-Scale Datasets," in *Data Mining for Scientific and Engineering Applications*, R. Grossman, C. Kamath, P. Kegelmeyer, V. Kumar, and R. Namburu, eds., Kluwer, 2001.

Journal Papers

P. Joisha and P. Banerjee*, "The efficient computation of ownership sets in HPF," *IEEE Trans. Parallel and Distributed Systems*, vol. 12, no. 8, Aug. 2001.

A. Choudhary*, M. Kandemir, J. No, G. Memik, X. Shen, W. Liao, H. Nagesh, S. More, V. Taylor*, R. Thakur, and R. Stevens, "Data management for large-scale scientific computations in high-performance distributed systems," *Cluster Computing*, vol. 3, pp. 45–60, 2000.

S. Goil and A. Choudhary*, “PARSIMONY: An infrastructure for parallel multidimensional analysis and data mining,” *J. Parallel and Distributed Computing*, *Special Issue on High-Performance Data Mining*, vol. 61, no. 3, March 2001.

M. Kandemir, A. Choudhary*, P. Banerjee*, J. Ramanujam, and N. Shenoy, “Minimizing data and synchronization costs in one-way communication,” *IEEE Trans. Parallel and Distributed Systems,* vol. 11, no. 12, pp. 1232–1251, Dec. 2000.

M. Kandemir, J. Ramanujam, and A. Choudhary*, “Compiler algorithms for optimizing locality and parallelism on shared and distributed-memory machines,” *J. Parallel and Distributed Computing*, vol. 60, pp. 924–965, 2000.

N. Shenoy, A. Choudhary*, and P. Banerjee*, “An algorithm for synthesis of large time-constrained heterogeneous adaptive systems,” *ACM Trans. Design Automation of Electronic Systems*, vol. 6, no. 2, April 2001.

Y. I. Ismail*, E. G. Friedman, and J. L. Neves, “Repeater insertion in tree-structured inductive interconnects,” *IEEE Trans. Circuits and Systems II: Analog and Digital Signal Processing,* vol. 48, no. 5, pp. 471–481, May 2001.

Y. Massoud and Y. I. Ismail*, “On-chip inductance in high-speed integrated circuits,” invited paper, *IEEE Circuits and Devices Magazine*, vol. 17, no. 4, pp. 14–21, July 2001.

Invited Talks and Seminars

P. Banerjee*, “Overview of the MATCH Compiler for Compiling MATLAB Programs into Hardware,” *NASA Earth Sciences Technology Meeting*, Aug. 2001

A. Choudhary*, “Scalable Scientific Data Management,” keynote address, *Conf. on High-Speed Computing*, Gleneden Beach, OR, April 2001.

A. Choudhary*, “Power Aware Compilation and Synthesis,” Jet Propulsion Laboratory, June 2001.

Symposium Papers and Presentations

P. Banerjee*, M. Haldar, A. Nayak, and A. Choudhary*, “Overview of the MATCH compiler for compiling MATLAB programs into hardware,” *NASA Earth Science Technology Conf.,* Washington, DC, Aug. 2001.

D. Chakrabarti and P. Banerjee*, “Global optimization techniques for automatic parallelization of hybrid applications,” *Int. Conf. Supercomputing*, Sorrento, Italy, June 2001.

P. Joisha and P. Banerjee*, “Correctly detecting intrinsic type errors in typeless languages such as MATLAB,” *APL Conf.,* New Haven, CT, June 2001.

A. K. Jones and P. Banerjee*, “Parallel implementation of matrix and signal processing libraries on FPGAs,” *IASTED Parallel and Distributed Computing Systems Conf. (PDCS 2001)*, Anaheim, CA, Aug. 2001.

V. Kim, P. Banerjee*, K. De, and J. Brouwers, “Parallel and distributed VLSI synthesis for commercial CAD on a network of workstations,” *12th IASTED Int. Conf. Parallel and Distributed Computing Systems (PDCS 2000),* Las Vegas, NV, Nov. 2000.

A. Nayak, M. Haldar, P. Banerjee*, C. Chen, and. M. Sarrafzadeh, “Power optimization of delay-constrained circuits,” *Application Specific Integrated Circuit / System-on-a-Chip Conf. (ISCI/SOC 2000)*, Washington, DC, Sept. 2000.

N. Shenoy, P. Banerjee*, A. Choudhary*, and M. Kandemir, “Efficient synthesis of array-intensive computations onto FPGA-based accelerators,” *VLSI Design Conf.,* Bangalore, India, Jan. 2001.

Y. Yuan and P. Banerjee*, “Comparative study of parallel algorithms for 3-D capacitance extraction on distributed-memory multiprocessors,” *Int. Conf. Computer Design (ICCD’2000)*, Austin, TX, Sept. 2000.

M. Haldar, A. Nayak, A. Choudhary*, and P. Banerjee*, “Scheduling algorithms for automated synthesis of pipelined designs on FPGAs for applications described in MATLAB,” *Int. Conf. Compilers, Architectures and Synthesis for Embedded Systems (CASES 2000)*, San Jose, CA, Nov. 2000.

M. Haldar, A. Nayak, A. Choudhary*, and P. Banerjee*, “Automated synthesis of pipelined designs on FPGAs for signal and image processing applications described in MATLAB,” *Asia Pacific Design Automation Conf. (ASP-DAC)*, Tokyo, Japan, Feb. 2001.

M. Haldar, A. Nayak, A. Choudhary*, and P. Banerjee*, “FPGA hardware synthesis from MATLAB utilizing optimized IP cores,” *9th ACM SIGDA Int. Symp. Field Programmable Gate Arrays*, San Jose, CA, Feb. 2001.

M. Haldar, A. Nayak, N. Shenoy, A. Choudhary*, and P. Banerjee*, “FPGA hardware synthesis from MATLAB,” *VLSI Design Conf.,* Bangalore, India, Jan. 2001.

W. Liao, X. Shen, and A. Choudhary*, “Meta-data management system for high-performance large-scale scientific data access,” *7th Int. Conf. High-Performance Computing*, Dec. 2000.

S. More and A. Choudhary*, “Scheduling queries for tape-resident data,” *European Conf. Parallel Computing*, 2000.

A. Moshovos, G. Memik, and A. Choudhary*, “JETTY: Reducing snoop-induced power consumption in small-scale, bus-based SMP systems,” *7th Int. Symp. High-Performance Computer Architecture*, Monterrey, Mexico, Jan. 2001.

A. Nayak, M. Haldar, A. Choudhary*, and P. Banerjee*, “Precision and error analysis of MATLAB applications during automated hardware synthesis for FPGAs,” *Design Automation and Test in Europe (DATE 2001)*, Berlin, Germany, March 2001.

A. Nayak, M. Haldar, A. Choudhary*, and P. Banerjee*, “Parallelization of MATLAB applications for a multi-FPGA system,” *FPGA Symp. Custom Computing Machines (FCCM-2001),* Napa Valley, CA, April 2001.

X. Shen, W. Liao, and A. Choudhary*, “Remote I/O optimization and evaluation for tertiary storage systems through storage resource broker,” *IASTED Applied Informatics*, Innsbruck, Austria, Feb. 2001.

X. Shen, W. Liao, and A. Choudhary*, “An integrated graphical user interface for high-performance distributed computing,” *Int. Database Engineering and Applications Symp. (IDEAS)*, Grenoble, France, July 2001.

Y. I. Ismail* and E. G. Friedman, “Fast and accurate simulation of tree-structured interconnects,” *IEEE Midwest Symp. Circuits and Systems*, Aug. 2000.

Y. I. Ismail*, E. G. Friedman, and J. L. Neves, “Exploiting on-chip inductance in high-speed clock distribution networks,” *IEEE Midwest Symp. Circuits and Systems*, Aug. 2000.

Y. I. Ismail*, E. G. Friedman, and J. L. Neves, “Exploiting on-chip inductance in high-speed clock distribution networks,” *IEEE Workshop Signal Processing Systems,* Oct. 2000.

M. H. Masud, S. Hsien, and Y. I. Ismail*, “Circuit and physical level challenges in SoC circuits,” invited paper, *IEEE World Multi-Conf. Systemics, Cybernetics and Informatics*, June 2001 (Best Paper Award).

Ph.D. Dissertations

Malay Haldar, *Optimized Hardware Synthesis for FPGAs* (2001, co-advisors: P. Banerjee* and A. Choudhary*)

Anshuman Nayak, *Automatic Parallelization and Optimizations for Synthesizing MATLAB Programs on Multi-FPGA Systems* (2001, co-advisors: P. Banerjee* and A. Choudhary*)

Xiaohui Shen, *Large-Scale Data Management for Scientific Computing* (2001, advisor: A. Choudhary*)