

VLSI Design and CAD, 1999–2000



Externally Funded Research Projects

CHIMAERA: Architecture, Compilers, and Configuration Management for Reconfigurable Computing for Mass-Market Computing

P. Banerjee*, S. Hauck, and M. Sarrafzadeh*

Sponsor: Defense Advanced Research Projects Agency

This research project seeks to develop a complete adaptive solution for general-purpose computing systems. It includes research in adaptive computer architectures, configuration-management techniques, high-level compilation, mapping algorithms, template-based physical design, software / algorithms optimized for adaptive systems, and defense applications of adaptive computing. A key specific aim is to produce a general-purpose computing paradigm simple enough to become the standard mass-market computing model, yet with enough power to enable several orders-of-magnitude speedup for defense applications. This will yield a future defense computing solution with the price and availability advantages of commercial off-the-shelf hardware.

MATCH: A MATLAB Compilation Environment for Adaptive Computing Systems

P. Banerjee* and A. N. Choudhary*

Sponsor: Defense Advanced Research Projects Agency

Adaptive computing systems constitute a new class of computing and communication technology composed of configurable hardware capable of system-level adaptation. Such systems are often built out of combinations of microprocessor-based embedded systems, specialized digital signal processors (DSP's), and field-programmable gate arrays (FPGA's). The objective of this project is to make it easier for users to develop efficient codes for adaptive computing systems. As part of this project, we are developing a compiler that allows input of a user's applications written in the high-level language, MATLAB, and generates efficient low-level code that runs on commercial off-the-shelf FPGA's, embedded processors, and DSP's.

*Denotes VLSI Design and CAD faculty member(s), listed in alphabetical order.

PACT: Power-Aware Architectural and Compilation Techniques

P. Banerjee*, M. Sarrafzadeh*, A. N. Choudhary*, A. Moshovos, and H. Yuen

Sponsor: Defense Advanced Research Projects Agency

The objective of the PACT Project is to develop power-aware architectural techniques and associated compiler and CAD tool support. The specific goals of the PACT project are:

- Develop novel architectural and compiler concepts at various levels that can reduce the total energy consumption in specific applications by factors of 10-100X over conventional, non-power-aware architectures.
- Develop compiler techniques to automate the process of generating efficient code that is within a factor of two of the best manual approach with respect to optimizing power under performance and resource constraints.
- Demonstrate the usefulness of the compiler and architectural concepts on some real applications.

We will target specific algorithms / applications that are of interest to DOD. Moreover, we will develop a prototype of a general-purpose memory system chipset to be used on a variety of systems and applications.

PANTHER: A High-Performance Distributed-Computing Infrastructure

P. Banerjee*, A. N. Choudhary*, M. Sarrafzadeh*, P. Scheuermann, and V. Taylor

Sponsor: National Science Foundation

Specific aims of this project include:

- Explore using high-speed networking and computing to investigate file-systems and data-management issues for high-performance distributed computing.
- Investigate the parallel-programming support of networks of high-speed workstations and personal computers as an alternative to stand-alone parallel computers.
- Investigate high-performance CAD of electronic systems in a heterogeneous environment.
- Develop a Web-based CAD computing center that takes advantage of high-speed networking.
- Explore new instructional techniques that take advantage of high bandwidth and high speed.

Algorithm Design for VLSI

M. Sarrafzadeh*

Sponsor: National Science Foundation

Performance-driven issues related to deep submicron geometries, reliability, and other factors make the VLSI placement problem a real challenge. Even the classical (area-minimization) placement problem is not completely understood. Previously, we demonstrated several issues that must be considered in designing a placement algorithm. We are building on this work to design a new class of placement algorithms called NRG. In addition to good placement algorithms, we need good predictors that can quickly estimate the placement cost function. We are working on methodologies for designing a good predictor. The main idea is to reduce the placement search space and then find a very fast placement in the reduced space. Placement results are good only if the subsequent routing step is made easy. We are working on integrated placement and routing approaches, adopting a hierarchical approach. Preliminary results show significant improvement over existing techniques.

Application Specific Processor Synthesis (ASPROS)

M. Sarrafzadeh*

Sponsor: Motorola Center for Communications

The goal of this project is to develop a methodology, hardware, and software support to make feasible the vision of a three-month design cycle for multimedia processors. We intend to circumvent ad-hoc analyses and development schemes, and provide the level of automation necessary to effectively search the design space and quickly generate the optimized variant. A key focus is parameterization, which circumvents redundant designs. We have identified a set of projects eventually leading to an optimized multimedia processor synthesis environment: (1) hardware design of a class of micro-sequencers with varying performance and functionality; (2) development of a general methodology for parameterization of DSP-based data paths; and (3) development of a micro-sequencer-based hardware-software partitioner for the control part of the design.

Mapping Time Oriented Tools for Logic Emulation

S. Hauck and M. Sarrafzadeh*

Sponsor: National Science Foundation (matching funds from AT&T and Northwestern University)

The goal of this research is to develop fast mapping tools and architectures for logic emulations that can greatly reduce the mapping time, and thus radically improve the speed and usefulness of logic emulation. We are developing technology mapping tools that integrate decomposition and covering. Further, we are developing placement tools that use partitioning methods to do higher-quality global placement. Combined, these will improve both the mapping times and resulting quality of FPGA-based implementations. Routing complexity estimators are also being developed to guide algorithm choice, exploiting the mapping time / quality tradeoffs in many techniques. We are also considering new FPGA architectures for logic emulators, developing systems that can support much faster mapping times and yet still achieve high-quality results. By integrating all of these steps together, we are creating a complete mapping-time oriented tool suite for logic emulation which can exploit the mapping time / quality tradeoff in these systems.

Book Section / Chapter

M. Kandemir, J. Ramanujam, A. Choudhary*, and P. Banerjee*, "An Iteration Space Transformation Algorithm Based on Explicit Data Layout Representation for Optimizing Locality," in *Languages and Compilers for Parallel Computers*, S. Chatterjee et al., eds., *Lecture Notes in Computer Science*, Springer-Verlag, 1999.

Journals Edited

P. Banerjee*, Assoc. Editor, *IEEE Trans. Computers*.

P. Banerjee*, Assoc. Editor, *IEEE Trans. Parallel and Distributed Systems*.

P. Banerjee*, Assoc. Editor, *J. Parallel and Distributed Computing*.

A. N. Choudhary*, Assoc. Editor, *IEEE Trans. Parallel and Distributed Systems*.

A. N. Choudhary*, Subject Area Editor, *J. Parallel and Distributed Computing*.

M. Sarrafzadeh*, Assoc. Editor, *ACM Trans. Design Automation of Electronic Systems*.

Journal Papers

- M. Kandemir, P. Banerjee*, A. N. Choudhary*, J. Ramanujam, and N. Shenoy, "A global communication optimization technique based on data flow analysis and linear algebra," *ACM Trans. Programming Languages and Systems*, vol. 21, no. 6, Nov. 1999.
- A. Lain, D. Chakrabarti, and P. Banerjee*, "Compiler and run-time support for exploiting regularity within irregular applications," *IEEE Trans. Parallel and Distributed Systems*, vol. 11, no. 2, Feb. 2000.
- P. Prabhakaran and P. Banerjee*, "Parallel algorithms for force-directed scheduling of flattened and hierarchical signal flow graphs," *IEEE Trans. Computers*, 1999.
- A. N. Choudhary*, M. Kandemir, J. No, G. Memik, X. Shen, W. Liao, H. Nagesh, S. More, V. Taylor, R. Thakur, and R. Stevens, "Data management for large-scale scientific computations in high performance distributed systems," *Cluster Computing: The Journal of Networks, Software Tools and Applications*, vol. 3, no. 1, 2000, pp. 45–60.
- A. N. Choudhary*, W. Liao, D. Weiner, P. Varshney, R. Linderman, M. Linderman, and R. Brown, "Design, implementation and evaluation of parallel pipelined STAP on parallel computers," *IEEE Trans. Aerospace and Electronic Systems*, vol. 36, no. 2, April 2000, pp. 528–548.
- K. Bazargan and M. Sarrafzadeh*, "Fast template based placement for reconfigurable computing systems," special issue on Reconfigurable Computing, *IEEE Design & Test*, Jan.-March 2000, pp. 68–83.
- M. Enos, S. Hauck, and M. Sarrafzadeh*, "Evaluation and optimization of replication algorithms for logic replication," *IEEE Trans. Computer-Aided Design*, vol. 18, no. 9, Sept. 1999, pp. 1237-1248.

Symposium Sessions Organized / Chaired

- M. Sarrafzadeh*, Member, Program Committee, *IEEE Int. Conf. on Computer Aided Design (ICCAD'99)*, San Jose, CA, Nov 7-11, 1999.
- M. Sarrafzadeh*, General Co-Chairman, *2000 Great Lakes Symp. on VLSI (GLSVLSI'2000)*, Chicago, IL.
- M. Sarrafzadeh*, Member, Steering and Program Committees, *Workshop on System Level Interconnect Prediction (SLIP'2000)*, San Diego, CA.
- M. Sarrafzadeh*, Member, Program Committee, *2000 Southwest Symp. on Mixed-Signal Design*, San Diego, CA, Feb. 28-29, 2000.
- M. Sarrafzadeh*, Member, Steering Committee, *Int. Symp. on Quality of Electronic Design (ISQED'2000)*, San Jose, CA, March 21-22, 2000.
- M. Sarrafzadeh*, Member, Program Committee, and Chair, Steering Committee, *Int. Symp. on Physical Design*, San Diego, CA, April 2000.

Invited Talks and Seminars

- P. Banerjee*, "MATCH: A MATLAB Compilation Environment for Adaptive Computing Systems," *Texas A&M University*, ECE Dept. Distinguished Lecture, March 2000.
- P. Banerjee*, "PROPERCAD: Parallel Algorithms for VLSI CAD," *Texas A&M University*, ECE Dept. Distinguished Lecture, March 2000.

- P. Banerjee*, "A MATLAB Compilation Environment for Adaptive Computing Systems," *Illinois Institute of Technology*, Chicago, IL, ECE Dept. Outstanding Lecture, April 2000.
- P. Banerjee*, "A MATLAB Compilation Environment for Adaptive Computing Systems," *University of California-Irvine*, Computer and Information Science Dept. Distinguished Lecture, June 2000.
- P. Banerjee*, "A MATLAB Compilation Environment for Adaptive Computing Systems," *University of Toronto*, ECE Dept. Distinguished Lecture, Aug. 2000.
- A. N. Choudhary*, "High-Performance Data Management for Large-Scale Scientific Computing," Lawrence-Livermore National Laboratory, Livermore, CA, Jan. 2000
- M. Sarrafzadeh*, "Modern Physical Design: Algorithm, Technology and Methodology," *ICCAD'99* (full day tutorial).
- M. Sarrafzadeh* and M. Wang, "Interaction Among Cost Function During Placement," *Int. Conf. on VLSI and CAD*, Seoul, Korea, Oct. 26-29, 1999.
- J. Cong and M. Sarrafzadeh*, "Incremental Physical Design," *Int. Symp. on Physical Design (ISPD'2000)*.
- J. Cong, O. Coudert, and M. Sarrafzadeh*, "Incremental CAD," *ICCAD'2000* (embedded tutorial).
- A. Farrahi, D. Hathaway, M. Wang, and M. Sarrafzadeh*, "Quality of EDA CAD Tools: Definitions, Metrics and Directions," *ISQED'2000*, San Jose, CA, March 2000.
- A. Kahng and M. Sarrafzadeh*, "Modern Physical Design," *ICCAD'2000* (tutorial).

Symposium Papers

- P. Banerjee*, N. Shenoy, A. N. Choudhary*, S. Hauck, M. Haldar, P. Joisha, A. Jones, A. Kanhere, A. Nayak, S. Periyacheri, M. Walkden, and D. Zaretsky, "A MATLAB compiler for distributed heterogeneous reconfigurable computing systems," *Proc. Int. Symp. on FPGA Custom Computing Machines (FCCM-2000)*, Napa Valley, CA, April 2000.
- P. Joisha and P. Banerjee*, "Efficient computation of ownership sets in HPF," *Proc. Languages and Compilers for Parallel Computing (LCPC-2000)*, Yorktown Heights, NY, Aug. 2000.
- P. Joisha, A. Kanhere, P. Banerjee*, N. Shenoy, and A. N. Choudhary*, "Handling context-sensitive syntactic issues in the design of a front-end for a MATLAB compiler," *Proc. ACM Array Programming Languages Conf. (APL-Berlin-2000)*, Berlin, Germany, July 24–27, 2000.
- V. Kim, P. Banerjee*, and K. De, "Fine-grained parallel VLSI synthesis for commercial CAD on a network of workstations," *Proc. Int. Conf. on Parallel Processing (ICPP-2000)*, Toronto, Canada, Aug. 2000.
- A. Nayak, P. Banerjee*, C. Chen, and M. Sarrafzadeh*, "Power optimization issues in dual voltage design," *Proc. Int. Conf. on Design Automation (ICDA 2000)*, Beijing, China, Aug. 21–25, 2000.
- Z. Ye, P. Banerjee*, S. Hauck, and A. Moshovos, "CHIMAERA: A high-performance architecture with a tightly-coupled reconfigurable functional unit," *Proc. 27th Int. Symp. on Computer Architecture*, Vancouver, Canada, June 10–14, 2000.
- Z. Ye, N. Shenoy, and P. Banerjee*, "A C compiler for a processor with a reconfigurable functional unit," *Proc. ACM/SIGDA Symp. on Field Programmable Gate Arrays*, Monterey, CA, Feb. 2000.
- Y. Yuan and P. Banerjee*, "A parallel 3-D capacitance extraction program," *Proc. 6th Int. Conf. on High Performance Computing (HiPC'99)*, Calcutta, India, Dec. 1999.

- Y. Yuan and P. Banerjee*, "A parallel implementation of a fast multipole based 3-D capacitance extraction program on distributed memory multicomputers," *Proc. 14th Int. Parallel and Distributed Processing Symp. (IPDPS 2000)*, Cancun, Mexico, May 1–5, 2000 (Best Paper Award).
- M. Haldar, A. Nayak, A. Choudhary*, and P. Banerjee*, "Parallel algorithms for FPGA placement," *Proc. Great Lakes Symp. on VLSI (GVLSI 2000)*, Chicago, IL, March 2000.
- M. Haldar, A. Nayak, A. Kanhere, P. Joisha, N. Shenoy, A. Choudhary*, and P. Banerjee*, "MATCH virtual machine: An adaptive runtime system to execute MATLAB in parallel," *Proc. Int. Conf. on Parallel Processing (ICPP-2000)*, Toronto, Canada, Aug. 2000.
- M. Kandemir, A. N. Choudhary*, and J. Ramanujam, "I/O-conscious tiling for disk-resident data sets," *Proc. 5th Int. Euro-Par Conf. on Parallel Processing (Euro-Par'99)*, Toulouse, France, Aug.-Sept. 1999.
- M. Kandemir, A. N. Choudhary*, and J. Ramanujam, "Compiler optimizations for I/O-intensive computations," *Proc. 1999 Int. Conf. on Parallel Processing (ICPP'99)*, Aizu, Japan, Sept. 1999, pp. 164–171.
- M. Kandemir, A. N. Choudhary*, J. Ramanujam, and P. Banerjee*, "A framework for interprocedural locality optimization using both loop and data layout transformations," *Proc. 1999 Int. Conf. on Parallel Processing (ICPP'99)*, Aizu, Japan, Sept. 1999, pp. 95–102.
- M. Kandemir, A. N. Choudhary*, J. Ramanujam, and P. Banerjee*, "On reducing false sharing while improving locality on shared memory multiprocessors," *Proc. 1999 Int. Conf. on Parallel Architectures and Compilation Techniques (PACT'99)*, Newport Beach, CA, Oct. 12-16, 1999.
- W. Liao, A. N. Choudhary*, D. Wiener, and P. Varshney, "I/O implementation and evaluation of parallel pipelined STAP on high performance computers," *Proc. 6th Int. Conf. on High Performance Computing (HIPC'99)*, Calcutta, India, Dec. 1999.
- W. Liao, A. N. Choudhary*, D. Wiener, and P. Varshney, "Design and evaluation of I/O strategies for parallel pipelined STAP applications," *Proc. Int. Parallel and Distributed Processing Symp.*, May 2000, pp. 655–662.
- G. Memik, M. Kandemir, and A. N. Choudhary*, "Design and evaluation of a compiler-directed I/O technique," *Proc. European Conf. on Parallel Computing (Euro-Par'2000)*, Munich, Germany, Aug. 2000.
- G. Memik, M. Kandemir, and A. N. Choudhary*, "Design and evaluation of smart disk architectures for commercial workloads," *Proc. Int. Conf. on Parallel Processing (ICPP 2000)*, Toronto, Canada, Aug. 21–24, 2000.
- G. Memik, M. Kandemir, A. N. Choudhary*, and V. Taylor, "APRIL: A run-time library for tape resident data," *Proc. 8th NASA Goddard Conf. on Mass Storage Systems and Technologies*, in cooperation with the *17th IEEE Symp. on Mass Storage Systems*, College Park, MD, March 27–30, 2000, pp. 61–75.
- S. More and A. N. Choudhary*, "Tertiary storage organization for large multidimensional datasets," *Proc. 8th NASA Goddard Space Flight Center Conf. on Mass Storage Systems and Technologies and 17th IEEE Symp. on Mass Storage Systems*, Baltimore, MD, March 2000.
- H. Nagesh, S. Goil, and A. N. Choudhary*, "PMAFIA: A scalable parallel subspace clustering algorithm for massive datasets," *Proc. Int. Conf. on Parallel Processing (ICPP'2000)*, Toronto, Canada, Aug. 21–24, 2000.

- A. Nayak, M. Haldar, A. Kanhere, P. Joisha, N. Shenoy, A. Choudhary*, and P. Banerjee*, "A library based compiler to execute MATLAB programs on a heterogeneous platform," *Proc. ISCA 13th Int. Conf. on Parallel and Distributed Computing Systems (PDCS-2000)*, Las Vegas, NV, Aug. 8–10, 2000.
- S. Periyacheri, A. Nayak, A. Jones, N. Shenoy, A. Choudhary*, and P. Banerjee*, "Library functions in reconfigurable hardware for matrix and signal processing operations in MATLAB," *Proc. 11th IASTED Parallel and Distributed Computing and Systems Conf. (PDCS'99)*, Cambridge, MA, Nov. 1999.
- X. Shen and A. N. Choudhary*, "A distributed multi-storage resource architecture and I/O performance prediction for scientific computing," *Proc. High Performance Distributed Computing Conf. (HPDC'2000)*, Pittsburgh, PA, Aug. 2000.
- X. Shen, W. Liao, A. N. Choudhary*, G. Memik, M. Kandemir, S. More, G. Thiruvathukal, and A. Singh, "A novel application development environment for large-scale scientific computations," *Proc. Int. Conf. on Supercomputing*, Santa Fe, NM, May 2000.
- X. Shen, G. Thiruvathukal, W. Liao, A. N. Choudhary*, and A. Singh, "A JAVA graphical user interface for large-scale scientific computations in heterogeneous systems," *Proc. 4th Int. Conf. on High Performance Computing –ASIA*, Beijing, China, May 2000.
- N. Shenoy, A. Choudhary*, and P. Banerjee*, "A system-level synthesis algorithm with guaranteed solution quality," *Proc. Design Automation and Test in Europe (DATE 2000)*, Paris, France, March 27–30, 2000.
- A. Srinilta and A. N. Choudhary*, "Multi-pool caching in continuous media server," *Proc. Conf. on Multimedia Modeling (MMM'99)*, Ottawa, Canada, Oct. 29, 1999, pp. 267–282.
- K. Bazargan, R. Kastner, S. Ogrenci, and M. Sarrafzadeh*, "A C to hardware / software compiler," *Proc. IEEE FCCM: Symp. on Field Programmable Custom Computing Machines*, Napa Valley, CA, April 21-23, 2000.
- K. Bazargan, A. Ranjan, and M. Sarrafzadeh*, "Fast and accurate estimation of floorplans in logic / high-level synthesis," *2000 Great Lakes Symposium on VLSI (GLSVLSI'2000)*, Chicago, IL, March 2-4, 2000, pp. 95–100.
- C. Chen and M. Sarrafzadeh*, "An exact algorithm for gate-level power-delay tradeoff using two voltages," *Proc. ICCD*, Oct. 1999.
- C. Chen and M. Sarrafzadeh*, "Provably good algorithm for low power consumption with dual supply voltages," *Proc. Int. Conf. on Computer-Aided Design (ICCAD'99)*, Nov. 7-10, 1999.
- C. Chen and M. Sarrafzadeh*, "Power reduction by simultaneous voltage scaling and gate sizing," *Proc. ASP-DAC'2000*, China.
- R. Kastner, K. Bazargan, and M. Sarrafzadeh*, "Physical design of reconfigurable computing systems with firm macros," *Proc. Workshop on Reconfigurable Computing (WoRC'99)*, Oct. 1999.
- R. Kastner, E. Bozorgzadeh, and M. Sarrafzadeh*, "Coupling aware routing," *ASIC/SOC*, Washington DC.
- S. Ogrenci, A. Katsaggelos, and M. Sarrafzadeh*, "FPGA analysis and implementation of image restoration," *FPGA'2000*, Monterey, CA, Feb. 10-11, 2000.
- A. Srivatsava, R. Kastner, and M. Sarrafzadeh*, "Gate duplication for performance optimization," *Int. Workshop on Logic Synthesis (IWLS'2000)*, Los Angeles, CA.
- M. Wang and M. Sarrafzadeh*, "Modeling and minimization of routing congestion," *Proc. ASP-DAC'2000*, China.

- M. Wang, S. Lim, J. Cong, and M. Sarrafzadeh*, "Multi-way partitioning using bi-partition heuristics," *Proc. ASP-DAC'2000*, China.
- M. Wang, X. Yang, K. Eguro, and M. Sarrafzadeh*, "Multi-center congestion minimization during placement," *Proc. Int. Symp. on Physical Design (ISPD'2000)*.
- M. Wang, X. Yang, K. Eguro, and M. Sarrafzadeh*, "A snap-on placement tool," *Proc. Int. Symp. on Physical Design (ISPD'2000)*.

Ph.D. Dissertations

- Dhruva Chakrabarti, *Compiler Support for Parallel Irregular Applications* (2000, advisor: P. Banerjee*)
- Yanhong Yuan, *Parallel Algorithms for 3D Resistance and Capacitance Extraction* (2000, advisor: P. Banerjee*)
- Kiarash Bazargan, *Algorithms for Reconfigurable Computing Work* (2000, advisor: M. Sarrafzadeh*)
- Maogang Wang, *Placement Algorithms in VLSI CAD* (2000, advisor: M. Sarrafzadeh*)