FD-TD Modeling of Digital Signal Propagation in 3-D Circuits With Passive and Active Loads

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Abstract—Most existing computer-aided circuit design tools are limited when digital clock speeds exceed several hundred MHz. These tools may not deal effectively with the physics of UHF and microwave electromagnetic wave energy transport along metal surfaces such as ground planes or in the air away from metal paths that are common at or above this frequency range. In this paper, we discuss full-wave modeling of electronic circuits in three dimensions using the finite-difference time-domain (FD-TD) solution of Maxwell's equations. Parameters such as stripline complex line impedance, propagation constant, capacitance per unit length and inductance per unit length can be easily computed as a function of frequency. We also discuss FD-TD Maxwell's equations computational modeling of lumped-circuit loads and sources in 3-D, including resistors and resistive voltage sources, capacitors, inductors, diodes, and transistors. We believe that this approach will be useful in simulating the large-signal behavior of very high-speed nonlinear analog and digital devices in the context of the full-wave time-dependent electromagnetic field.

I. INTRODUCTION

In the past, digital logic designers have not seriously considered the electromagnetic details of their systems. Clock speeds have been low enough and logic levels high enough that electromagnetic problems have been minor. But as voltage levels drop below one volt and clock speeds increase to 100 MHz and above, key electromagnetics issues must be addressed.

For example, most existing computer-aided circuit design tools (primarily SPICE) are limited at digital clock speeds exceeding 300 MHz. These tools do not deal with the physics of UHF/microwave electromagnetic wave energy transport along metal surfaces like ground planes, or in the air away from metal paths, that are common above this frequency. Effectively, electronic digital systems develop substantial analog wave effects when clock rates are high enough, with full-wave electromagnetic field phenomena markedly affecting the propagation, cross-talk, and radiation of electronic digital pulses in typical structures such as multilayer circuit boards and multichip modules. The general theme of this paper is that a synthesis of electromagnetic fields and waves and electronic

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circuit devices will eventually become necessary to design very high-speed digital systems.

The specific research summarized in this paper addresses numerical modeling of 3-D digital interconnects with passive and active loads directly from Maxwell's equations. We utilize the finite-difference time-domain (FD-TD) method, a simple, robust numerical technique for direct time integration of Maxwell's equations that has become the means to model a wide variety of electromagnetic wave problems [1]. Using the basic algorithm introduced by Yee [2], FD-TD implements the space derivatives of the curl operators via finite differences in regular interleaved (dual) Cartesian space meshes for the electric and magnetic fields. Simple leapfrog time integration is employed.

The literature indicates that 3-D FD-TD modeling of metallic digital interconnects has commenced. Liang *et al.* [3] modeled picosecond pulse propagation along co-planar waveguides above a gallium arsenide substrate. Shibata and Sano [4] modeled propagation along metal-insulator-semiconductor lines. Lam *et al.* [5] modeled digital signal propagation and radiation for VLSI packaging, and Maeda *et al.* [6] modeled digital pulse propagation through vias in a three-layer circuit board.

Work is also being done in FD-TD modeling of passive and active devices that can either source or terminate metallic transmission lines. Two groups reported incorporation of self-consistent models of charge transport into a 3-D FD-TD solver to model picosecond pulse generation by an optically excited gallium arsenide device: Sano and Shibata [7] with a drift-diffusion charge-transport model, and El-Ghazaly [8] with a Monte Carlo model. A third group Sui *et al.* [9], developed lumped-circuit models of typical passive and active circuit elements (resistors, inductors, capacitors, diodes, and transistors) incorporated into a 2-D FD-TD solver for exploring electromagnetic modeling of nanosecond-regime circuits.

The work of this paper follows directly from [6] and [9]. In Section III, we illustrate the power of FD-TD modeling to deduce a classical electromagnetic compatibility problem, ground loop current flow, in what may be the most complex 3-D passive circuit model so far, a module consisting of a stack of multilayer circuit boards penetrated by scores of via pins. Using a uniform space resolution of 0.004 inch, each layer, via, and pin of every circuit board was modeled. 60-million vector field unknowns were solved per modeling run, a factor of perhaps 100 times larger than the capacity of the largest SPICE or finite-element CAD tool available.

In Section IV, we improve and extend the work of [9] to 3-D, introducing a semi-implicit algorithm that permits analog to the curl of \bar{H} observed at $E_z|_{i,j,k}$ as the large-signal behavior of nonlinear circuit devices to be simulated in a numerically stable manner in the context of the FD-TD Maxwell's equations solver. We report FD-TD electromagnetic wave models of the resistor, resistive voltage source, capacitor, inductor, diode, and bipolar junction transistor.

II. FD-TD Algorithm and Extension

A. Basic FD-TD Formulation

The derivation of the basic FD-TD equations used to solve Maxwell's equations has been documented extensively [1], [2], [10] so it will not be repeated. In all of the cases to be discussed, a uniform, 3-D Cartesian Yee mesh is used with a unit cell of dimensions $\Delta x, \Delta y, and \Delta z$. Numerical stability is maintained by bounding the time step [11].

Consider Maxwell's curl Hequation, suitable for timestepping the electric field

$$\nabla \times \overline{H} = \overline{J}_c + \frac{\partial \overline{D}}{\partial t}$$
 (1a)

where the electric conduction current is $\overline{J}_c = \sigma \overline{E}$ and the electric displacement is $\overline{D} = \varepsilon \overline{E}$. Using central differencing with the standard Yee subscript/superscript notation for space and time coordinates, respectively, (1a) becomes

$$E_{z}|_{i,j,k}^{n+1} = \left(\frac{1 - \frac{\sigma_{i,j,k}\Delta t}{2\epsilon_{i,j,k}}}{1 + \frac{\sigma_{i,j,k}\Delta t}{2\epsilon_{i,j,k}}}\right) E_{z}|_{i,j,k}^{n}$$

$$+ \left(\frac{\frac{\Delta t}{\epsilon_{i,j,k}}}{1 + \frac{\sigma_{i,j,k}\Delta t}{2\epsilon_{i,j,k}}}\right) \left(\frac{\frac{H_{y}|_{i+1/2,j,k}^{n+1/2} - H_{y}|_{i-1/2,j,k}^{n+1/2}}{\Delta x} + \frac{\Delta x}{1 + \frac{\sigma_{i,j,k}\Delta t}{2\epsilon_{i,j,k}}}\right) \left(\frac{H_{x}|_{i,j-1/2,k}^{n+1/2} - H_{x}|_{i,j+1/2,k}^{n+1/2}}{\Delta y}\right)$$
(1b)

An important observation is that all H quantities on the right-hand side of (1b) are at time step n + 1/2, centered in time relative to the stored electric field, $E_z|_{i,j,k}^n$, and the newly updated electric field, $E_z|_{i,j,k}^{n+1}$. Further, the bracketed coefficients are derived assuming that J_c is also evaluated at time step n + 1/2, taking

$$J_{c}|_{i,j,k}^{n+1/2} = \sigma_{i,j,k} E_{z}|_{i,j,k}^{n+1/2} = \frac{\sigma_{i,j,k}}{2} (E_{z}|_{i,j,k}^{n} + E_{z}|_{i,j,k}^{n+1})$$
(2a)

We denote this as the "semi-implicit formulation" for the conduction current in that this current relies in part upon the updated electric field to be determined as a result of the timestepping, and yet does not result in a system of simultaneous equations. This results in a numerically stable algorithm for arbitrary positive values of σ [1], [10].

For convenience in the discussions of this paper, we shall assume that all circuit components are located in a freespace region ($\epsilon = \epsilon_o, \sigma = 0, J_C = 0$). Additional notational convenience is provided by denoting the Yee finite-difference

$$\nabla \times H_{i,j,k}^{n+1/2} = \frac{H_y \Big|_{i+1/2,j,k}^{n+1/2} - H_y \Big|_{i-1/2,j,k}^{n+1/2}}{\Delta x} + \frac{H_x \Big|_{i,j-1/2,k}^{n+1/2} - H_x \Big|_{i,j+1/2,k}^{n+1/2}}{\Delta y}$$
(2b)

Then, (1b) can be rewritten very simply as

$$E_z|_{i,j,k}^{n+1} = E_z|_{i,j,k}^n + \frac{\Delta t}{\epsilon_o} \nabla \times H|_{i,j,k}^{n+1/2}.$$
 (2c)

B. Extended FD-TD Formulation

The electric field time-stepping algorithm is now modified to allow for the addition of lumped linear and nonlinear circuit elements. The basis of this formulation, reported in [9] for 2-D problems, showed that lumped circuit elements can be accounted for in Maxwell's equations by adding a lumped electric current density term, J_L , to the conduction and displacement currents on the right hand side of (1a). Equation (1a) now becomes

$$\nabla \times \overline{H} = \overline{J}_c + \frac{\partial \overline{D}}{\partial t} + \overline{J}_L. \tag{3a}$$

We assume that a lumped element is located in free-space at the field $E_z|_{i,j,k}$; is z-oriented in the grid; and provides a local current density that is related to the total element current, I_L , as

$$J_L = \frac{I_L}{\Delta x \Delta y}.$$
 (3b)

Here, I_L is possibly a time-derivative, time-integral, scalar multiple, or nonlinear function of the electric potential, V = $E_z|_{i,j,k}\Delta z$, developed across the element. Note that the assumed positive direction of I_L is +z. Then, the following modified version of (2c) suffices to specify the presence of the lumped circuit element in the electromagnetic field grid

$$E_z|_{i,j,k}^{n+1} = E_z|_{i,j,k}^n + \frac{\Delta t}{\epsilon_o} \nabla \times H|_{i,j,k}^{n+1/2} - \frac{\Delta t}{\epsilon_o \Delta x \Delta y} I_L^{n+1/2}. \tag{4}$$

In the key departure from the work of [9], we have defined in (4) the lumped current as being evaluated at the mid time step, n+1/2, just as we did in (2a) for the conduction current. Since the lumped current is a function of the electric field at the circuit element, this requires averaging the values of $E_z|_{i,j,k}^{n+1}$ and $E_z|_{i,j,k}^n$, an operation that yields a numerically-stable semiimplicit time-stepping algorithm. Generalization of all of this to x and y orientations of a lumped element is straightforward by permuting the coordinate subscripts of the field quantities.

III. INTERCONNECT GEOMETRIES WITHOUT LUMPED LOADS

A. Parallel Coplanar Microstrips

Preliminary studies were performed to establish the validity of FD-TD results for characteristic impedance and delay of parallel co-planar microstrips. The first studies were done by

¹Note added in proof. See also Tsuei et al. [16]. for an independent expansion of the work of [9] to 3-D.

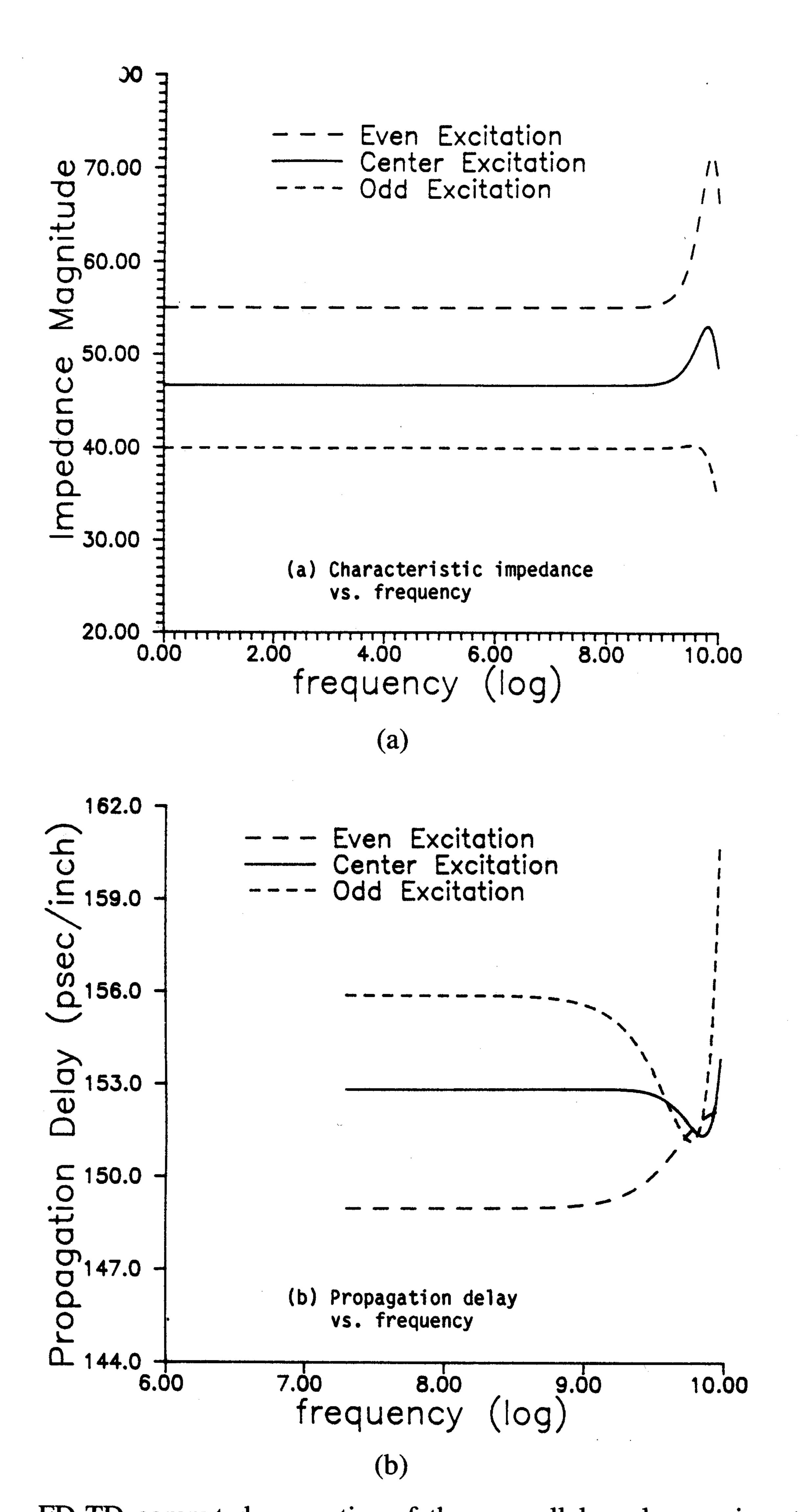


Fig. 1. FD-TD computed properties of three parallel coplanar microstrips: (a) characteristic impedance versus frequency; (b) propagation delay versus frequency.

setting up FD-TD grids for single x-directed microstrips of negligible metalization thickness and a variety of widths over dielectric substrates in the order of 1 mil (0.001 inch) thick. Grid cell size δ for these cases was in the order of 0.1 mil with Δt in the order of 4.2 fs. In all cases, conductors were "on grid," i.e., located at planar loci of tangential E components in the FD-TD mesh that were set to zero for all time steps, and with zeroed tangential E components on the conductor edges.

Mur absorbing boundary conditions [12] were set up at the outer lattice planes. To effectively decouple the Mur boundaries from the localized fields within and near the microstrip geometries, the FD-TD space lattice extended at least 20 free-space cells beyond the microstrip structures in all directions.

Excitation of a microstrip was provided by specifying a Gaussian-pulse time history for a group of co-linear electric field components (usually E_z) bridging the gap between the ground plane and the strip conductor at the desired source location. The characteristic impedance, Z_0 , of the microstrip was then found by forming the ratio of the discrete Fourier transforms of the line voltage and current, V and I, obtained

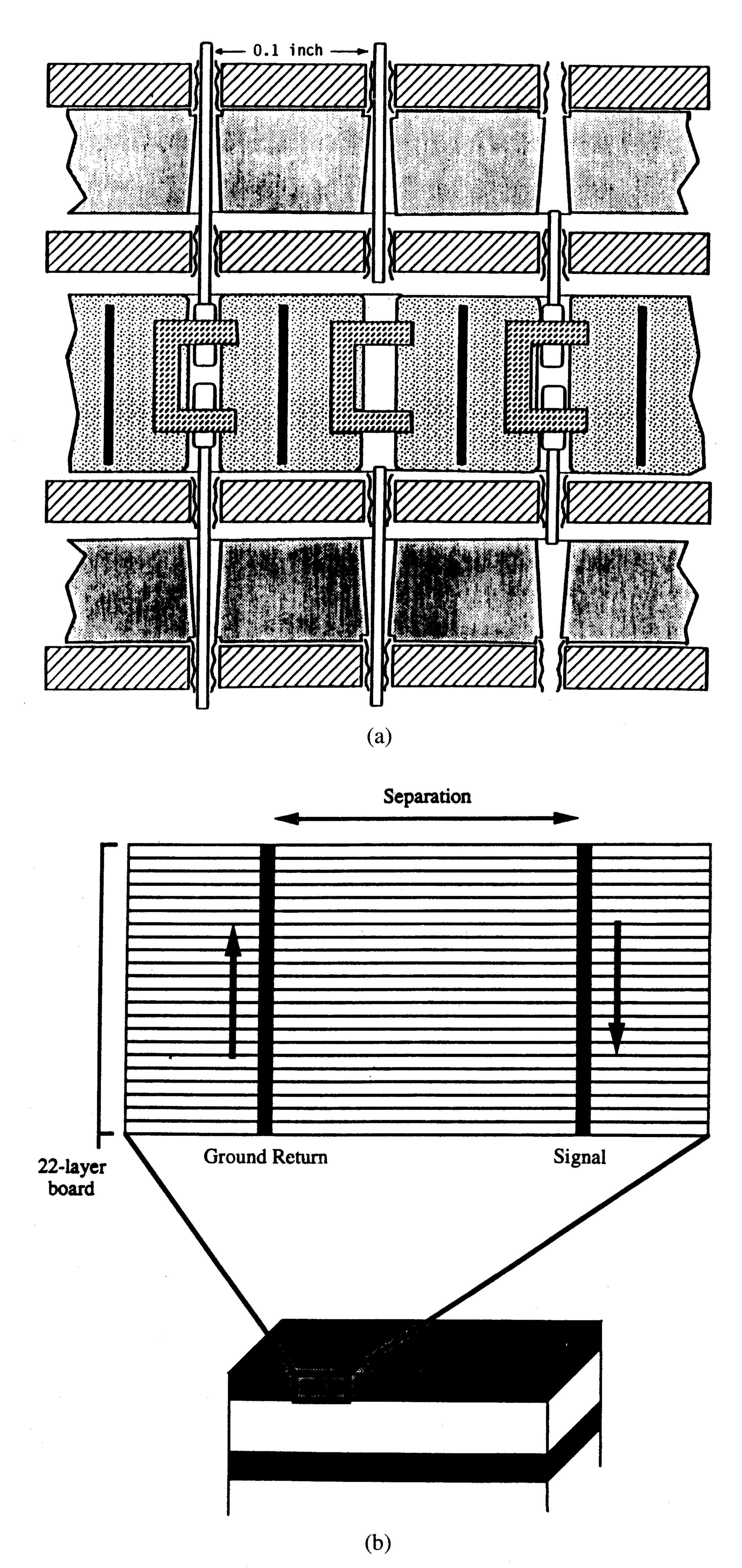


Fig. 2. 3-D connector module: (a) stack of four multilayer circuit boards perforated by scores of vertical via pins spaced on 0.1-inch centers; (b) generic sketch of digital signal and ground return paths in the top multilayer circuit board.

from the resulting propagating E and H fields:

$$V(t, x_i) = \int_{C_V} \overline{E}(t, x_i) \cdot d\overline{l}, \qquad I(t, x_i) = \oint_{C_I} \overline{H}(t, x_i) \cdot d\overline{l}$$

$$Z_0(\omega, x_i) = \mathcal{F}[V(t, x_i)] / \mathcal{F}[I(t, x_i)]. \tag{5}$$

Here, the contour path for V extends from the ground plane to the microstrip, while the contour path for I for extends around the strip conductor at its surface. This method showed the FD-TD computed values of Z_0 to be virtually independent

of frequency up to 1.0 GHz, and in the order of 1% agreement with textbook values [13].

Next, using similar FD-TD grid resolutions, we considered single microstrips with finite metalization thickness, possibly fully embedded within a dielectric layer. Here, FD-TD predictions were compared to measurements. In one example, a 1.1-mil-thick, 1.4-mil-wide metal strip was assumed to be suspended 1.1 mils above a large ground plane within a 3.1-mil-thick dielectric layer having $\varepsilon_r=3.2$. The FD-TD numerical simulation predicted a flat characteristic impedance, Z_0 , of 48 Ω up to 1.0 GHz, agreeing with the experimental results to within the measurement uncertainty (about 0.2 Ω). The computed variation of Z_0 above 1 GHz was found to be ± 2 Ω . Similar excellent agreement was found for the propagation delay, where the experimental value was 150.5 \pm 1.5 psec/inch, while the FD-TD prediction was 149.5 psec/inch.

We then studied the impedance and propagation delay of three parallel, co-planar microstrips having finite metalization thickness. Each microstrip had the geometry discussed above and was separated by 3.6 mils from the adjacent line(s). Even-mode results were obtained with all three strips excited simultaneously with the same polarity, while odd-mode results were obtained with the two outer strips excited with the opposite polarity relative to the center strip. Results were also observed for the center strip excited with the two outer strips floating. Fig. 1 shows Z_0 and the propagation delay predicted by FD-TD for all three cases. These results were obtained with $\delta = 0.1$ mil, $\Delta t = 4.2$ fs, and a lattice size of 200 \times 134 \times 42 cells. It is clear from the results that signal propagation on adjacent lines significantly influences the effective impedance of the line, and to a lesser degree affects the propagation delay. The FD-TD results were confirmed by laboratory studies which showed an approximate 7 Ω elevation of the characteristic impedance for the even-mode excitation, and an approximate 7 Ω reduction of the impedance for the oddmode excitation (both from dc to about 1 GHz). At frequencies approaching 10 GHz, the evolution of non-transmission-line modes within the trio of parallel lines suffices to progressively disturb the observed Z_0 and propagation delay.

B. Multilayered Interconnect Modeling Example

This section illustrates the power of FD-TD modeling to investigate a classical electromagnetic compatibility problem, ground loop current flow. In what may be the most complex 3-D passive circuit modeled by any means so far, we constructed a high-resolution FD-TD model of sub-nanosecond digital pulse propagation and crosstalk behavior in a real-world computer module consisting of a stack of four multilayer printed circuit boards (each with >10 metal-dielectric-metal layers) penetrated by scores of via pins forming a connector. A uniform space cell size of $\delta=4$ mils was used with time step $\Delta t=169$ fs. The space cell was the thickness of a single layer in the circuit boards, and 1/3 the diameter of each 12-mil-diameter circular via. In this manner, each layer, via, and pin of every circuit board and every connector was modeled in the final simulation, resulting in almost 60-million

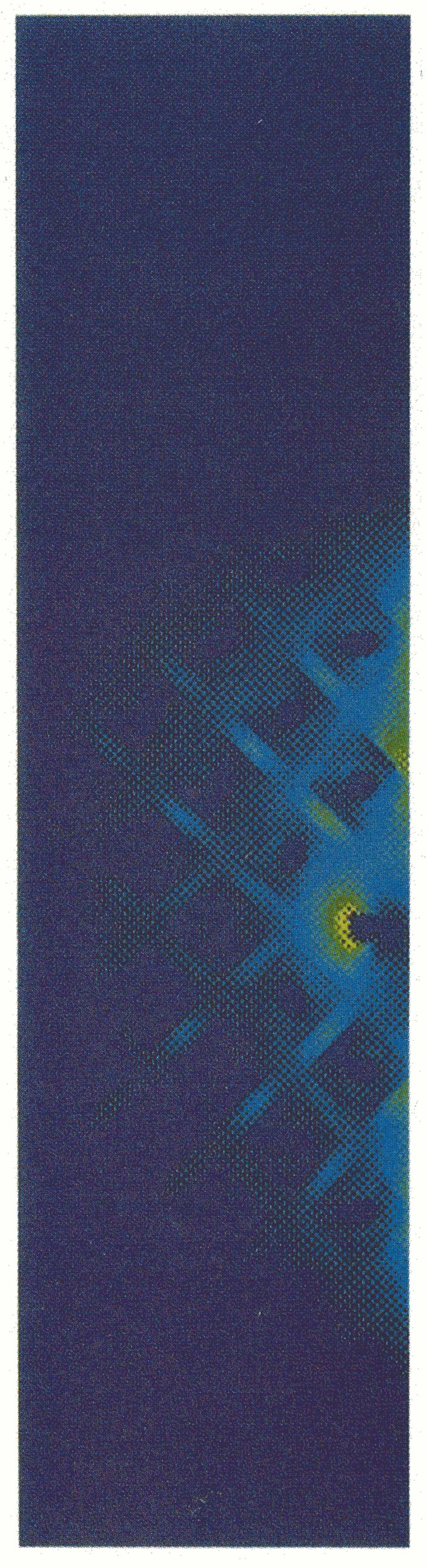


Fig. 3. Color plate showing the plan view of an outwardly propagating electromagnetic wave within the top multilayer circuit board generated by the passage of a subnanosecond pulse down a single vertical via pin. Color scale: yellow = maximum; green = moderate; dark blue = negligible.

vector field unknowns solved. Fig. 2(a) is a diagram of the full connector module, where each multilayer circuit board is shown as a cross-hatched horizontal slab. Vertical via pins located on 0.1-inch centers penetrate the stack of boards and connectors throughout the module. Fig. 2(b) is a generic sketch of a digital signal path and a ground-return path in the top multilayer circuit board.

Single Multilayer Circuit Board, Early Time Response: The first step in the study was to model in detail the early-time response of the top multilayer circuit board to an impulse of current (90-ps Gaussian pulse, spectral width about 20 GHz) propagating down a single vertical via pin. The via pin (in the circular via hole) was excited by pulsing a vertical electric field component, E_z , in the FD-TD lattice just above the pin

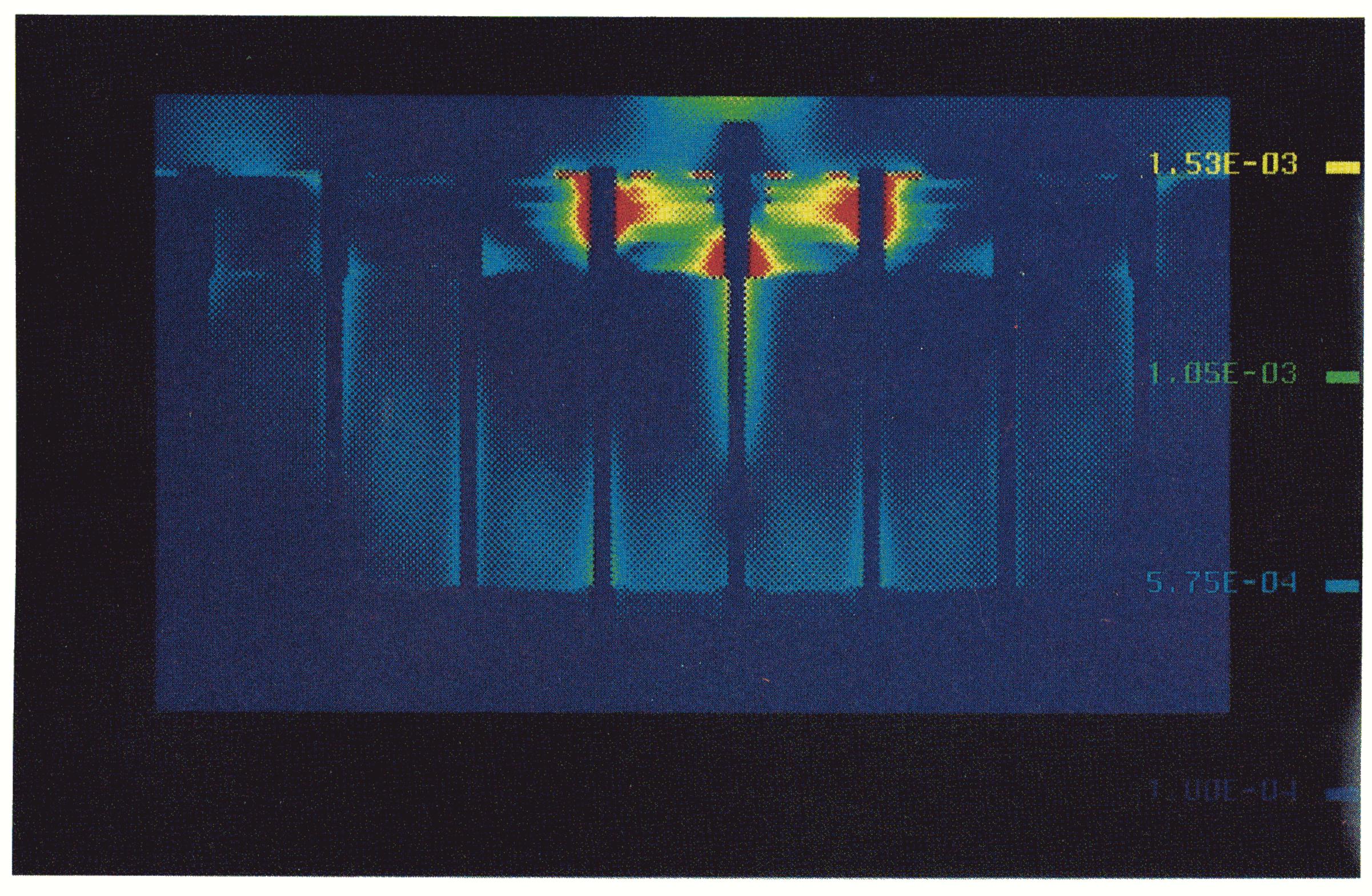


Fig. 4. Color plate of the early-time coupling of magnetic fields from the excited via pin to the adjacent unexcited via pins as seen in a vertical cut through the top multilayer board and connector of the stack of Fig. 2. Color scale: red = maximum; yellow = moderate; green = low-level; dark blue = negligible.

and below a simulated ground strap connected to the outer via pins designated as ground returns. The short duration of the pulse was selected primarily to permit time resolution of layer-to-layer pulse reflection effects within the circuit board. We utilized a $300 \times 92 \times 52$ cell FD-TD grid having 1.44 million cells (8.6 million unknowns, 19 MW of memory). Using a single processor of a Cray YMP-8, this grid size required 0.36 sec per time step. The power and signal metalizations of the circuit board were assumed to be infinitely thin.

Fig. 3 is a color plate showing the plan view of |H| of the outwardly propagating electromagnetic wave within the board generated by the passage of the pulse down the via pin. Although the relatively intense magnetic field adjacent to the excited via (shown by the yellow color) is quite localized, moderate-level magnetic fields (shown by light blue) emanate throughout the entire transverse cross section of the board and link *all* of the adjacent via pins, shown as dark dots in a diamond pattern. The complete color video of the dynamics of this phenomenon shows repeated bursts of outward propagating waves linking all points within transverse cross sections of the board as the pulse passes vertically through the multiple metal-dielectric-metal layers of the board. The resulting pin-to-pin cross-talk is vividly illustrated in the color plate of Fig. 4, which depicts $|\overline{H}|$ in a vertical cut through the top multilayer board and connector of the stack of Fig. 2. The coupling of magnetic fields from the excited via pin to the adjacent unexcited via pins is clearly indicated.

Complete Four-Board Connector Module, Late Time Response: The final step in the study was to model the response of the complete four-board connector module to the impulsive excitation of a single vertical via pin. Keeping the same space

resolution as for the single-board model, we enlarged the FD-TD grid to $300 \times 92 \times 340$ cells to contain the three additional multilayer circuit boards and connectors. The new grid totalled 9.4 million cells with 56 million vector field unknowns, and required 117 MW of memory. Using a single processor of a Cray YMP-8, this grid required 2.13 sec per time step, or 71 minutes for a complete run of 2000 time steps. (Using all eight of the Cray YMP processors reduced the running time by almost 8:1 to only 9 minutes.) Again, all power and signal metalizations of the circuit boards were assumed to be infinitely thin.

Color videos of pulse propagation and crosstalk were constructed to illustrate these phenomena. Fig. 5 is a color plate showing the magnitude and direction of late-time currents flowing along the vertical cross section of the complete connector module of Fig. 2 for a subnanosecond pulse assumed to excite a single vertical via pin in the top multilayer board. The currents were calculated in a post-processing step by numerically evaluating the curl of the magnetic field obtained from the 3-D FD-TD model. The color red was selected to denote downward-directed current, while the color green was selected to denote upward-directed current. At the time of this visualization, current had proceeded down the excited via through all four boards and all three connectors. But, upwarddirected (green) current is seen to flow on the adjacent vias. This represents undesired ground-loop coupling to the circuits using these vias.

IV. INTERCONNECT GEOMETRIES WITH LUMPED LOADS

In this section, we report 3-D FD-TD modeling of the connection of linear and nonlinear lumped loads to microstrip

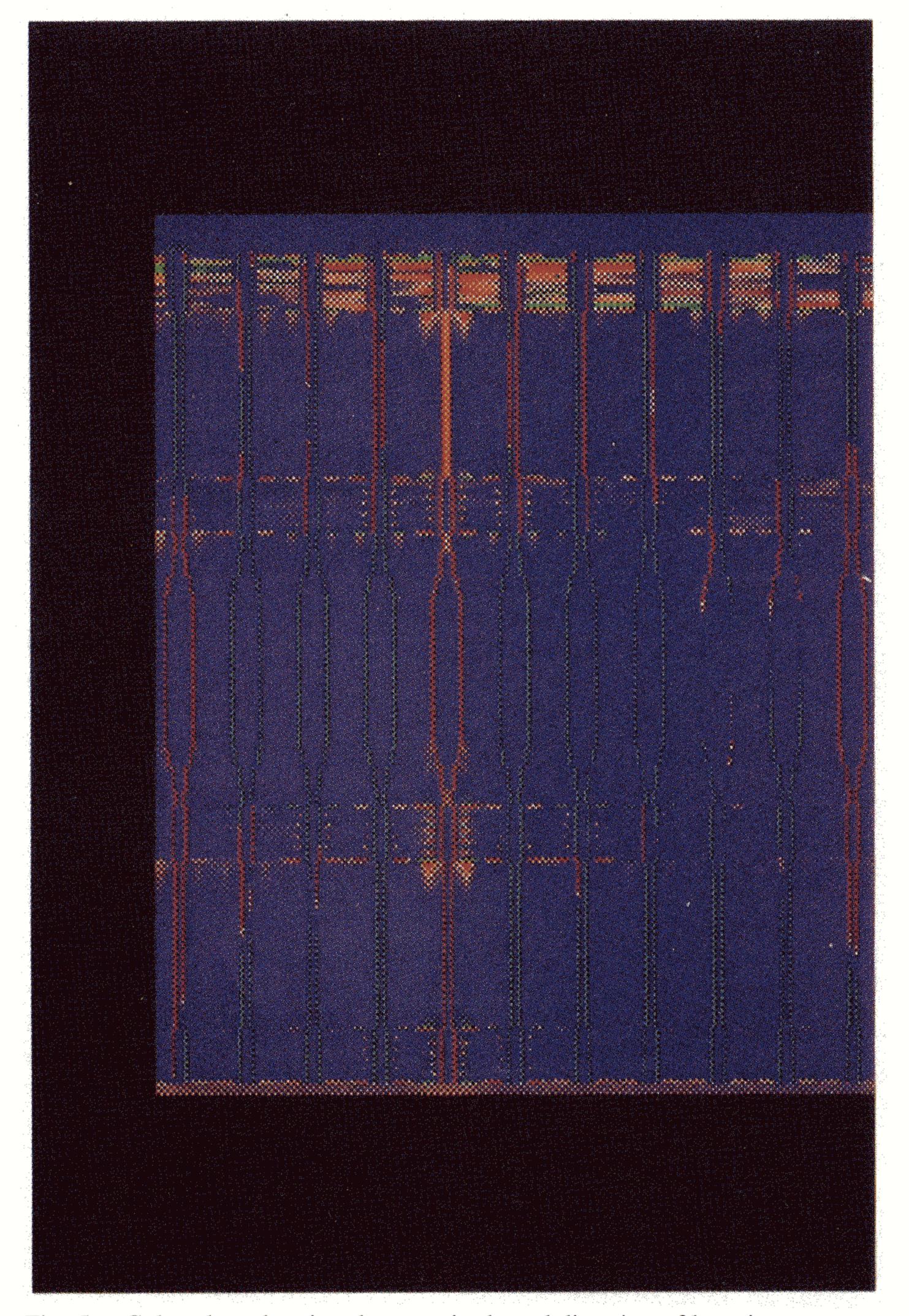


Fig. 5. Color plate showing the magnitude and direction of late-time currents flowing along the vertical cross section of the complete multiboard module of Fig. 2 for a subnanosecond digital pulse assumed to excite a single vertical via pin in the top multilayer board. Color scale: red = net downward-directed current; green = net upward-directed current; dark blue = negligible.

interconnects. Fig. 6 depicts the microstrip geometry considered. For convenience in the discussion, the microstrip is assumed to be oriented in the x-direction and the lumped load is assumed to be oriented in the z-direction. Extension of the theory to other Cartesian orientations in the FD-TD lattice is straightforward.

Lattice resolution δ in the range 1 to 8 mils was used in the simulations to study the effect of varying the number of cells spanning the strip conductor and the gap between it and the ground plane. For excitations with spectral components up to 1 GHz, the results were found to be only a very weak function of the grid space increment δ in this range. In all cases, conductors were "on grid," i.e., located at planar loci of tangential E components in the FD-TD lattice that were set to zero for all time steps, and with zeroed tangential E components on the conductor edges. Mur absorbing boundaries were used as specified in Section III.

A resistive source of the type discussed in Section B below was used in all of the FD-TD simulations of this section. The source resistance was matched to the line impedance so that retroreflections at the source were minimized.

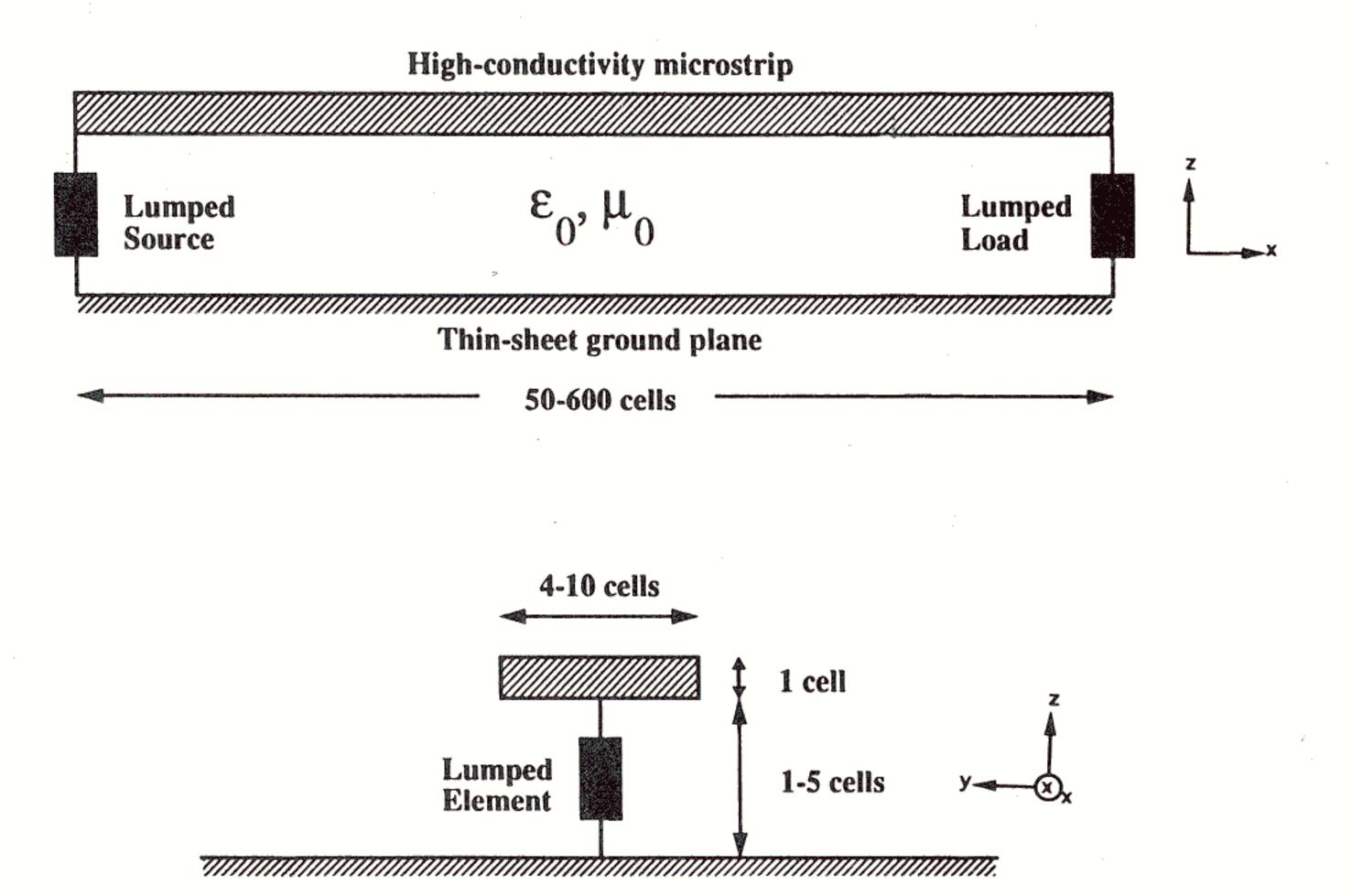


Fig. 6. Generic geometry used for 3-D FD-TD models of a linear or nonlinear lumped element terminating a stripline.

A. The Resistor

When studying microstrips it is very useful to have the capability to terminate the line in a resistive load, very likely matched to the characteristic impedance of the line. One method that we studied for terminating the line in an FD-TD grid is to insert a physical resistor block into the microstrip model using the relation $R = \rho L/A$ (where R is the desired resistance, ρ is the block's resistivity, and L and A represent the length and cross sectional area of the block) to select the parameters of the insert. The second method is to insert a numerical lumped element in an extension to 3-D of that described in [9]. Here, assuming a z-directed resistor located in free-space at the field component $E_z|_{i,j,k}$, the voltage-current characteristic that describes its behavior in a semi-implicit manner appropriate for stable operation of the FD-TD field solver is

$$I_{z}|_{i,j,k}^{n+1/2} = \frac{\Delta z}{2R} \left(E_{z}|_{i,j,k}^{n+1} + E_{z}|_{i,j,k}^{n} \right),$$

$$J_{L} = \frac{I_{z}|_{i,j,k}^{n+1/2}}{\Delta x \Delta y}$$
(6a)

where R is the value of the resistance and $\Delta x, \Delta y$ and Δz are the grid increments in the x,y and z directions. The corresponding time-stepping relation for $E_z|_{i,j,k}$ is

$$E_{z}|_{i,j,k}^{n+1} = \left(\frac{1 - \frac{\Delta t \Delta z}{2R\epsilon_{o} \Delta x \Delta y}}{1 + \frac{\Delta t \Delta z}{2R\epsilon_{o} \Delta x \Delta y}}\right) E_{z}|_{i,j,k}^{n} + \left(\frac{\frac{\Delta t}{\epsilon_{o}}}{1 + \frac{\Delta t \Delta z}{2R\epsilon_{o} \Delta x \Delta y}}\right) \nabla \times H|_{i,j,k}^{n+1/2}.$$
(6b)

To compare the impedance match provided by the physical and numerical resistors in the FD-TD mesh, we modeled a terminated 50- Ω transmission line similar to that of Section III-A excited by a 90-ps Gaussian pulse (spectral width of 20 GHz). After performing a discrete Fourier transform of the reflected pulse for each case, we found that both the physical and numerical resistors provided reflection coefficients of less than 1% up to 1 GHz. Fig. 7 shows the magnitude and phase of

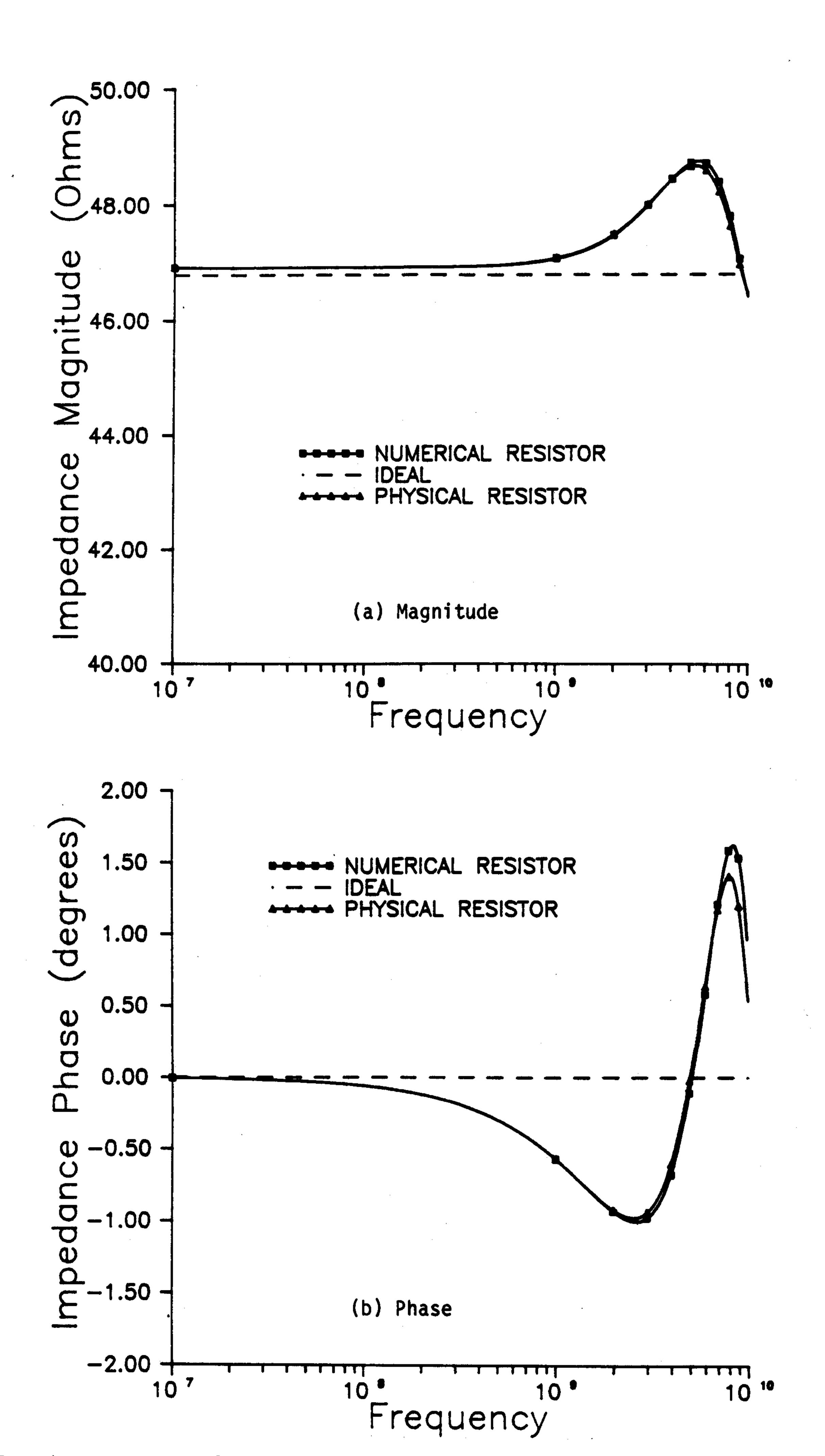


Fig. 7. Agreement of FD-TD computed effective load impedance (low frequency to 10 GHz) for the numerical resistor and the physical resistor: (a) magnitude; (b) phase.

the effective load impedance versus the ideal (matched) load impedance for the two cases. Over the span dc to 10 GHz, the maximum deviation is (positive $+2\Omega$, -0.5Ω) and $(+1.75^{\circ}$, -1°). The fact that the physical and numerical resistor results agree so well implies that the numerical resistor model does an excellent job of picking up the parasitic capacitance or inductance that may be present between the terminals of the physical resistor.

It is important to note that implementing (6b) at two adjacent electric field components between the microstrip signal line and ground plane simulates the presence of two parallel resistors terminating the line. The effective load resistance is thereby halved.

B. The Resistive Voltage Source

With the ability to model lumped elements in the context of FD-TD, it is a simple matter to model a nonreflecting (matched) source as a resistive voltage source in an extension to 3-D of that described in [9]. Again assuming a z-directed lumped element located in free-space at $E_z|_{i,j,k}$, the voltage-current characteristic that describes the behavior of a resistive

voltage source in a semi-implicit manner is

$$I_{z}|_{i,j,k}^{n+1/2} = \frac{\Delta z}{2R_{s}} \left(E_{z}|_{i,j,k}^{n+1} + E_{z}|_{i,j,k}^{n} \right) + \frac{V_{s}^{n+1/2}}{R_{S}},$$

$$J_{L} = \frac{I_{z}|_{i,j,k}^{n+1/2}}{\Delta x \Delta y}$$
(7a)

where $V_s^{n+1/2}$ is the source voltage and R_s is the internal source resistance. The corresponding time-stepping relation for $E_z|_{i,j,k}$ is

$$E_{z}|_{i,j,k}^{n+1} = \left(\frac{1 - \frac{\Delta t \Delta z}{2R_{S}\epsilon_{o}\Delta x \Delta y}}{1 + \frac{\Delta t \Delta z}{2R_{S}\epsilon_{o}\Delta x \Delta y}}\right) E_{z}|_{i,j,k}^{n}$$

$$+ \left(\frac{\frac{\Delta t}{\epsilon_{o}}}{1 + \frac{\Delta t \Delta z}{2R_{S}\epsilon_{o}\Delta x \Delta y}}\right) \nabla \times H|_{i,j,k}^{n+1/2}$$

$$+ \left(\frac{\frac{\Delta t}{R_{S}\epsilon_{o}\Delta x \Delta y}}{1 + \frac{\Delta t \Delta z}{2R_{S}\epsilon_{o}\Delta x \Delta y}}\right) V_{S}^{n+1/2}.$$

$$(7b)$$

C. The Capacitor

We next consider the insertion of a numerical lumped capacitor into the FD-TD grid in an extension to 3-D of that described in [9]. Again assuming a z-directed lumped element located in free-space at $E_z|_{i,j,k}$, the voltage-current characteristic that describes the capacitor's behavior in a semi-implicit manner is

$$I_{z}|_{i,j,k}^{n+1/2} = \frac{C\Delta z}{\Delta t} \left(E_{z}|_{i,j,k}^{n+1} - E_{z}|_{i,j,k}^{n} \right),$$

$$J_{L} = \frac{I_{z}|_{i,j,k}^{n+1/2}}{\Delta x \Delta y}$$
(8a)

where C is the value of the capacitance. This formulation differs from that of [9] in that the electric field samples are separated here by one time step rather than two. In this manner, we are consistent with the electric field sampling used for the numerical resistor described previously. The corresponding time-stepping relation for $E_z|_{i,i,k}$ is

$$E_{z}|_{i,j,k}^{n+1} = E_{z}|_{i,j,k}^{n} + \left(\frac{\frac{\Delta t}{\epsilon_{o}}}{1 + \frac{C\Delta z}{\epsilon_{o}\Delta x\Delta y}}\right)\nabla \times H|_{i,j,k}^{n+1/2}$$
(8b)

For the parallel combination of a capacitor, C, and resistor, R, located at $E_z|_{i,j,k}$, the results of (6a), (6b), (8a) and (8b) can be readily combined to yield the following time-stepping relation:

$$E_{z}|_{i,j,k}^{n+1} = \left(\frac{1 - \frac{\Delta t \Delta z}{2R\epsilon_{o}\Delta x \Delta y} + \frac{C\Delta z}{\epsilon_{o}\Delta x \Delta y}}{1 + \frac{\Delta t \Delta z}{2R\epsilon_{o}\Delta x \Delta y} + \frac{C\Delta z}{\epsilon_{o}\Delta x \Delta y}}\right) E_{z}|_{i,j,k}^{n} + \left(\frac{\frac{\Delta t}{\epsilon_{o}}}{1 + \frac{\Delta t \Delta z}{2R\epsilon_{o}\Delta x \Delta y} + \frac{C\Delta z}{\epsilon_{o}\Delta x \Delta y}}\right) \nabla \times H|_{i,j,k}^{n+1/2}.$$
(8c)

To test this FD-TD modeling approach, a variety of numerical capacitive loads were modeled at the end of a long (but ≈ 1 -mil scale in the transverse plane) 50Ω microstrip line subjected

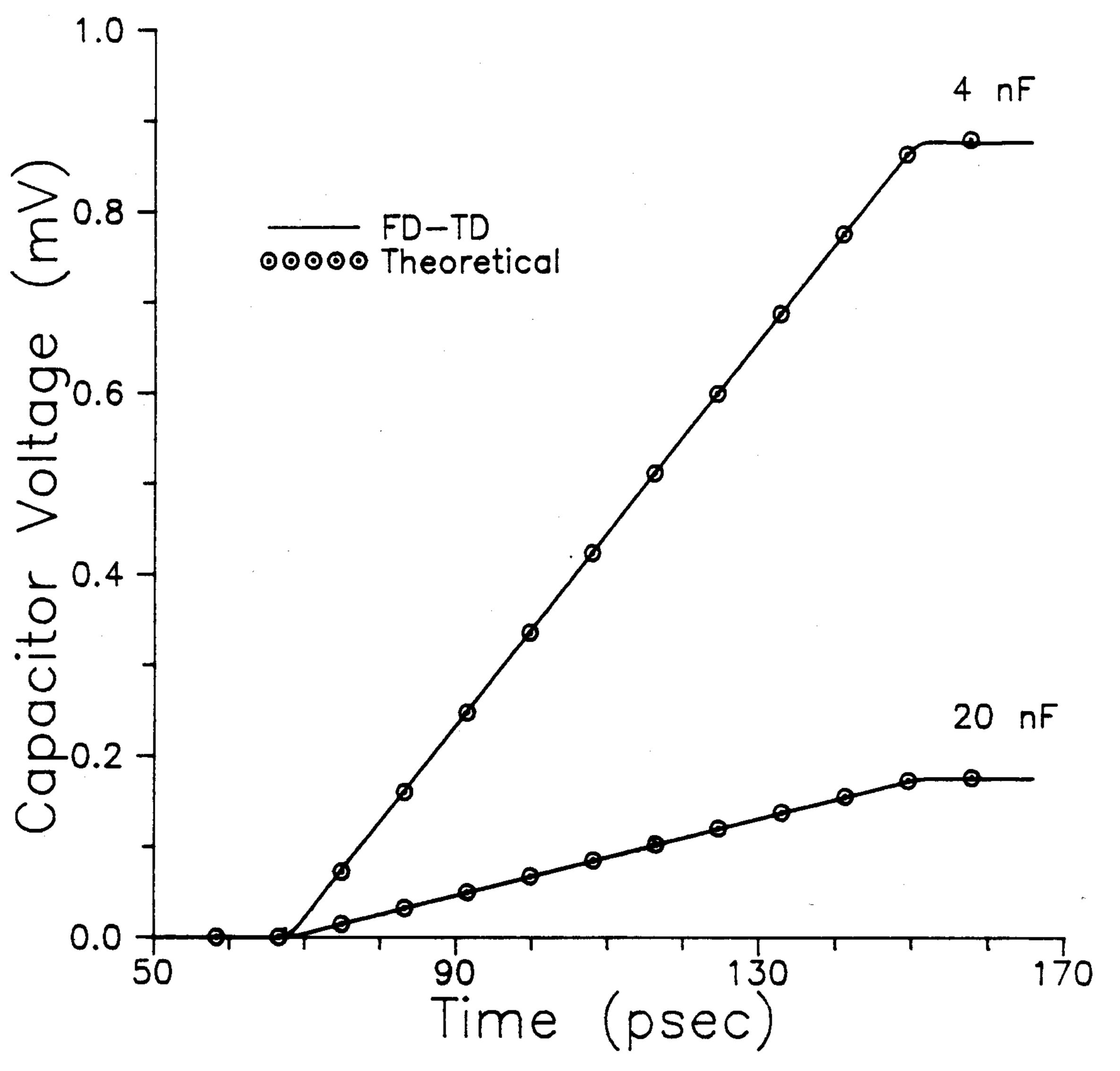


Fig. 8. Agreement of FD-TD and exact solutions for the voltage across the capacitor terminating the stripline for two values of the capacitor (stepwise incident pulse).

to a rectangular step-pulse excitation 1000 time steps long. The FD-TD computed voltage response vs. time across each capacitor was then compared to the exact theoretical response. Results are shown in Fig. 8 for microstrips terminated with 4 nF and 20 nF capacitors. The theoretical and FD-TD curves are indistinguishable.

D. The Inductor

We next consider the insertion of a numerical lumped inductor into the FD-TD grid in an extension to 3-D of that described in [9]. Again assuming a z-directed lumped element located in free-space at $E_z|_{i,j,k}$, the voltage-current characteristic that describes the inductor's behavior in a manner appropriate for stable operation of the FD-TD field solver is

$$I_{z}|_{i,j,k}^{n+1/2} = \frac{\Delta z \Delta t}{L} \sum_{m=1}^{n} E_{z}|_{i,j,k}^{m},$$

$$J_{L} = \frac{I_{z}|_{i,j,k}^{n+1/2}}{\Delta x \Delta y}$$
(9a)

where L is the value of the inductance. This formulation differs from that of [9] in that the electric field samples are summed only through time step n, which is consistent with the observation of the lumped current at time step n+1/2 that we employ throughout this development. The corresponding time-stepping relation for $E_z|_{i,i,k}$ is

$$E_{z}|_{i,j,k}^{n+1} = E_{z}|_{i,j,k}^{n} + \frac{\Delta t}{\epsilon_{o}} \nabla \times H|_{i,j,k}^{n+1/2}$$

$$- \frac{\Delta z(\Delta t)^{2}}{\epsilon_{o} L \Delta x \Delta y} \sum_{m=1}^{n} E_{z}|_{i,j,k}^{m}. \tag{9b}$$

E. The Diode

The current through a lumped-circuit diode is expressed by:

$$I_d = I_0 \left[e^{(qV_d/\mathbf{k}T)} - 1 \right] \tag{10}$$

where q is the charge of an electron, V_d is the voltage across the diode, k is Boltzmann's constant, and T is the temperature in degrees Kelvin. According to the 2-D study of [9], if one assumes a z-directed diode located in free-space at $E_z|_{i,j,k}$, the electric field time-stepping relation is given by

$$E_{z}|_{i,j,k}^{n+1} = E_{z}|_{i,j,k}^{n} + \frac{\Delta t}{\epsilon_{o}} \nabla \times H|_{i,j,k}^{n+1/2}$$

$$- \frac{\Delta t}{\epsilon_{o} \Delta x \Delta y} I_{0} \left[e^{\left(-qE_{z}|_{i,j,k}^{n} \Delta z/\kappa T\right)} - 1 \right]. \tag{11}$$

However, it has been determined that this expression yields a numerically unstable algorithm for diode voltages larger than 0.8 volts due to its explicit formulation which employs the previously computed electric field in the exponential.

We have found that a numerically stable FD-TD algorithm for the lumped diode can be realized in 3-D by using the semi-implicit update strategy for the electric field

$$E_z|_{i,j,k}^{n+1/2} = \frac{1}{2} \left(E_z|_{i,j,k}^{n+1} + E_z|_{i,j,k}^n \right). \tag{12}$$

In this manner, we obtain the following transcendental equation:

$$E_{z}|_{i,j,k}^{n+1} = E_{z}|_{i,j,k}^{n} + \frac{\Delta t}{\epsilon_{o}} \nabla \times H|_{i,j,k}^{n+1/2}$$

$$- \frac{\Delta t}{\epsilon_{o} \Delta x \Delta y} I_{0} \left\{ e^{\left[-q\left(E_{z}|_{i,j,k}^{n+1} + E_{z}|_{i,j,k}^{n}\right) \Delta z / 2\kappa T\right]} - 1 \right\}. \quad (13)$$

Upon solving (13) for the updated electric field using Newton's method, we find that the new model is numerically stable over a useful diode voltage range (up to 15 V).

To test this FD-TD modeling approach, a diode with a saturation current of 1×10^{-14} amps was modeled at the end of a 50 Ω microstrip line (of \approx 1-mil scale in the transverse plane). The excitation was a matched resistive voltage source providing a 10-volt, 200-MHz sinusoid. This high-level source was selected both to challenge the numerical stability of the FD-TD code and to test whether FD-TD can properly simulate driving a diode into hard clipping. As shown in Fig. 9, there is excellent agreement of the diode voltage response versus time as calculated by FD-TD and SPICE. No instability of the FD-TD solver was observed.

F. The Bipolar Junction Transistor

Reference [9] presented a 2-D FD-TD model for the linearized, small-signal behavior of a transistor. While good results were obtained using this model for selected parameters, some problems remained. This model is numerically unstable for extremely high or low values of the base resistance, r_b ; there is a problem with the fringing fields between the base and collector terminals; and the model lacks generality for large-signal and digital switching applications.

We have found a numerically stable FD-TD algorithm for the lumped NPN bipolar junction transistor (BJT) in 3-D that permits study of *large-signal* behavior, including digital switching. In the example considered here (Fig. 10), the BJT terminates a strip transmission line in a grounded-emitter configuration. The simulation is based upon a simple

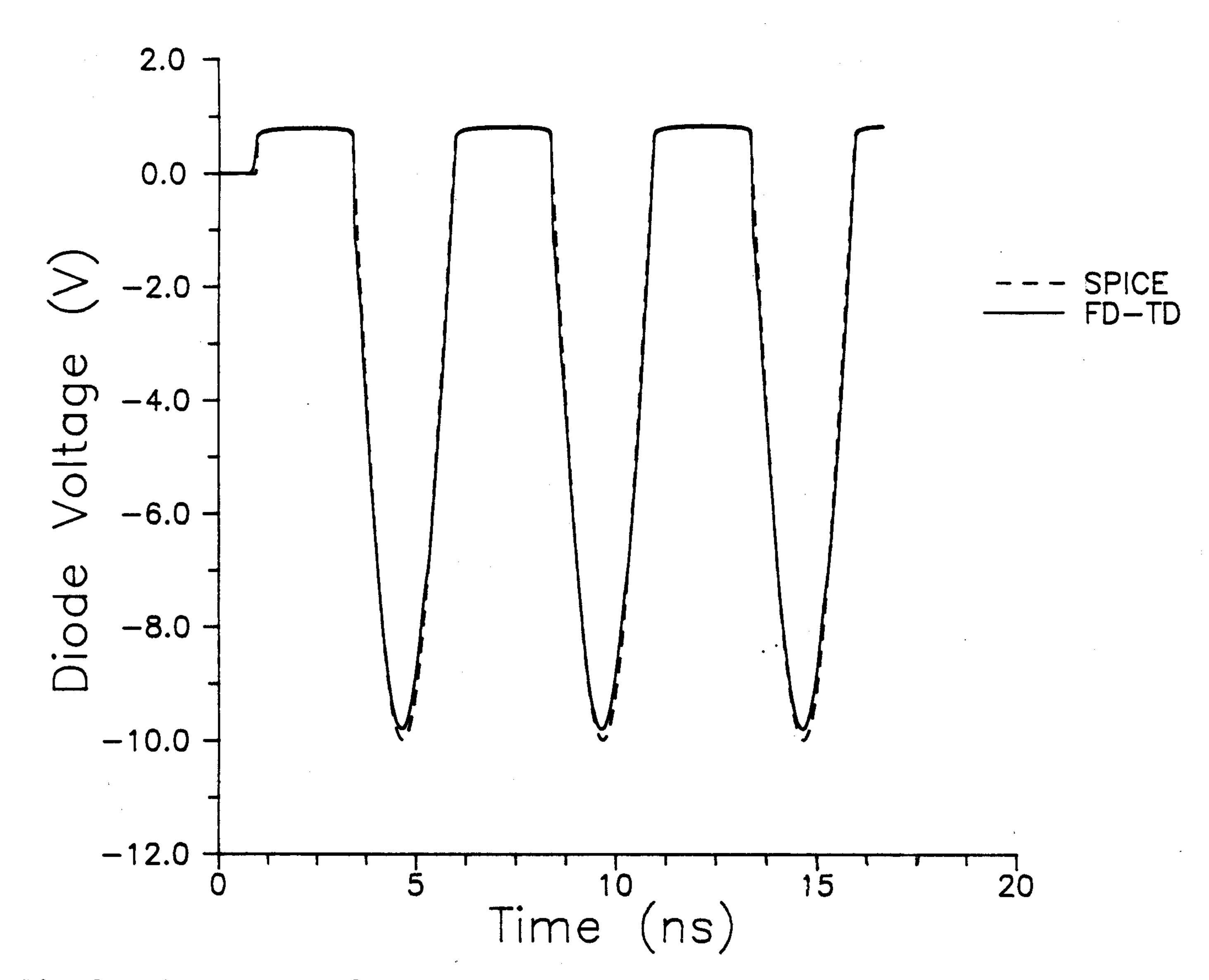


Fig. 9. Agreement of FD-TD and SPICE calculations for the voltage across the dio determinating the stripline.

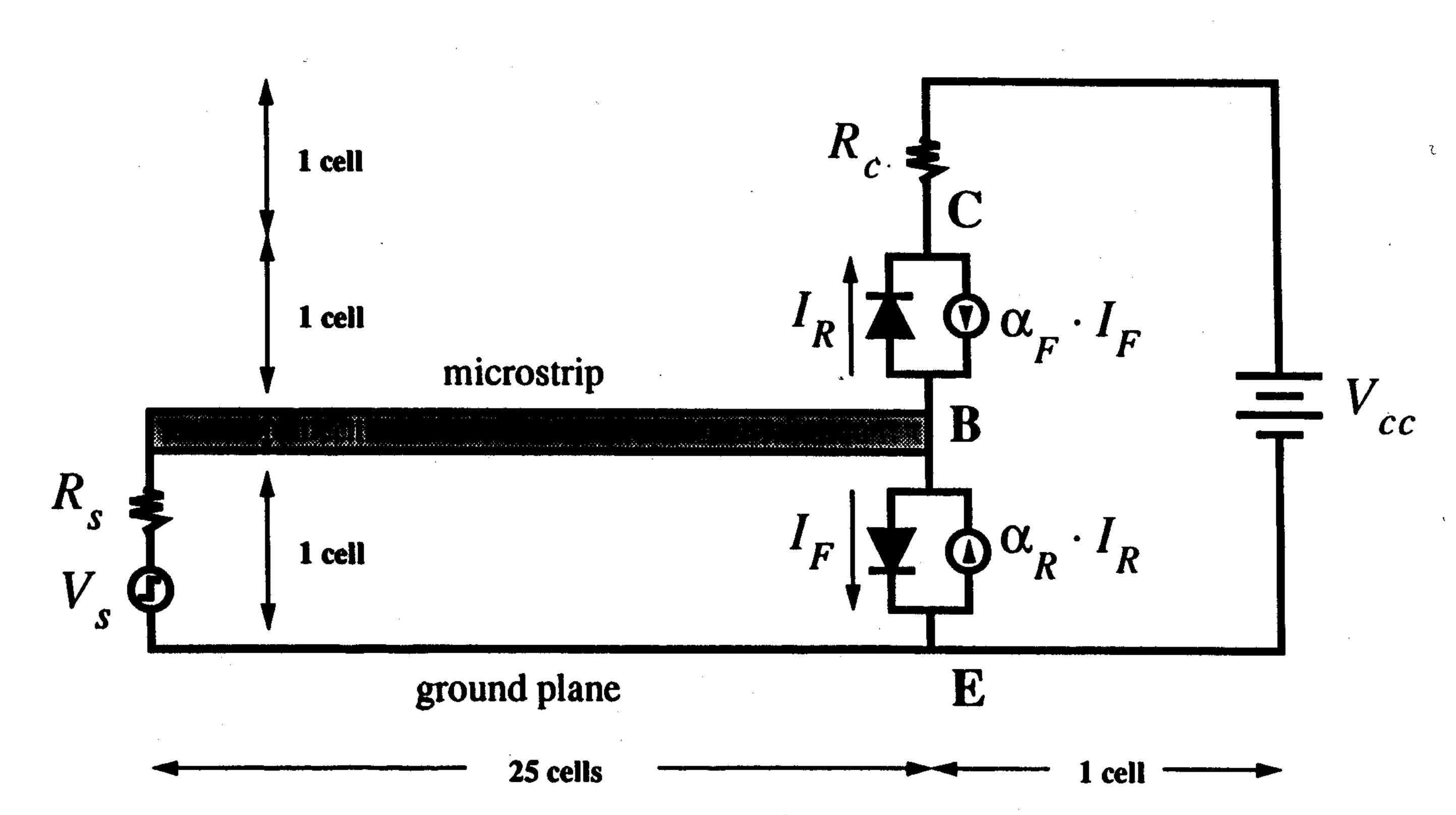


Fig. 10. Generic geometry used for 3-D FD-TD model of an NPN bipolar junction transistor (BJT) terminating a stripline in the common emitter configuration.

Ebers-Moll transistor model described by the following circuit equations [14]:

$$I_F = I_0 \left[e^{(qV_{\rm BE}/kT)} - 1 \right], \qquad I_R = I_0 \left[e^{(qV_{\rm BC}/kT)} - 1 \right],$$
(14)

$$I_E = \alpha_R I_R - I_F, \qquad I_C = I_R - \alpha_F I_F. \tag{15}$$

Now, assuming a transistor that is located in free-space and oriented in the z-direction in the FD-TD grid as shown in Fig. 10, we can use a semi-implicit strategy to express the base-emitter voltage, $V_{\rm BE}$, in terms of E_Z $|_{\rm EB}$, the FD-TD computed electric field in the one-cell gap between the ground plane and the end of the stripline

$$V_{\rm BE}^{n+1/2} = -\frac{\Delta z}{2} \left(E_Z|_{\rm EB}^{n+1} + E_z|_{\rm EB}^n \right). \tag{16}$$

A similar semi-implicit strategy is used to express the base-collector voltage, $V_{\rm BC}$, in terms of E_z $|_{\rm BC}$, the FD-TD computed electric field in the one-cell gap between the end of the stripline and the collector load:

$$V_{\rm BC}^{n+1/2} = \frac{\Delta}{2} \left(E_Z |_{\rm BC}^{n+1} + E_z|_{\rm BC}^n \right). \tag{17}$$

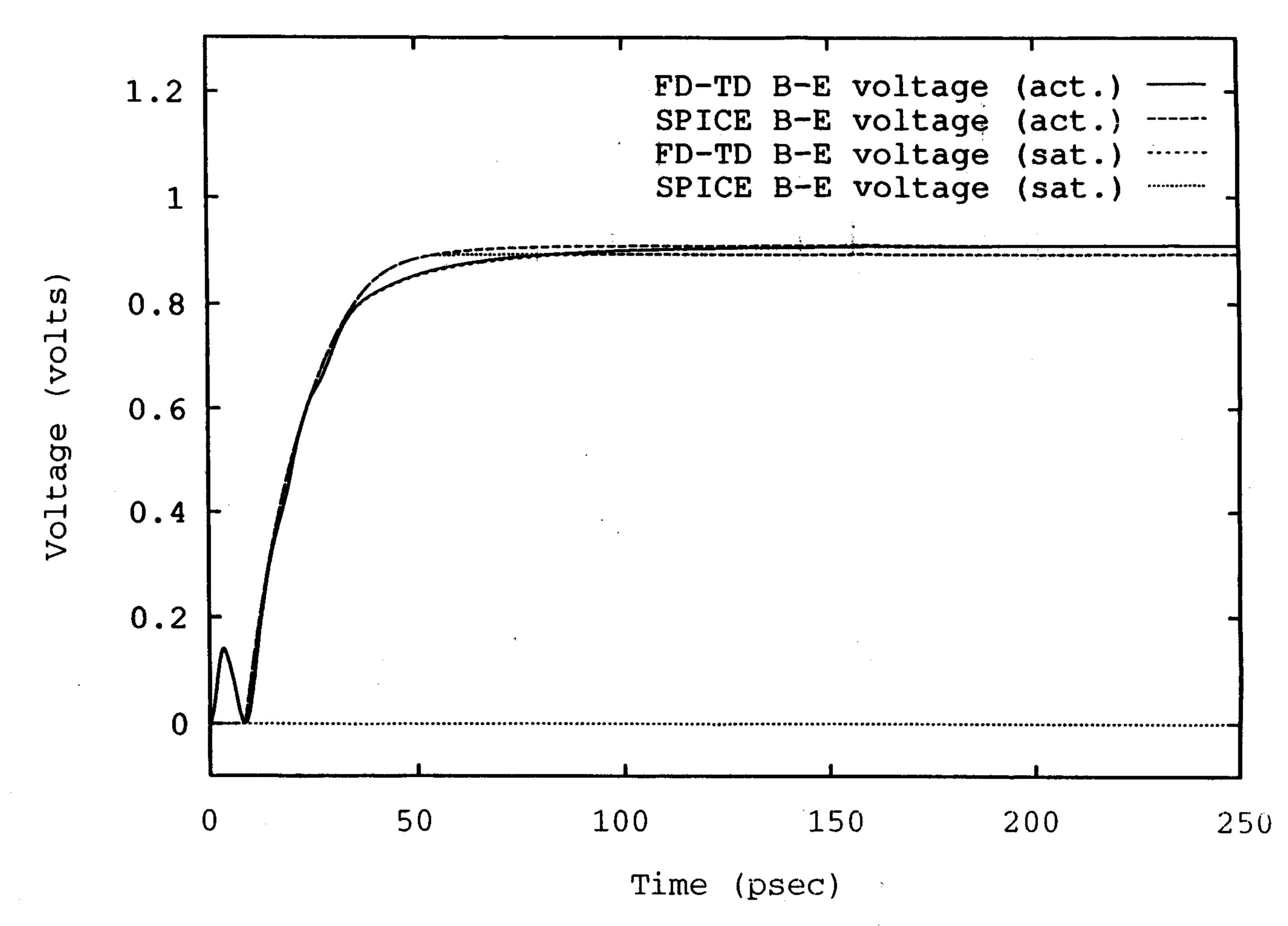


Fig. 11. Agreement of FD-TD and SPICE calculations for the transistor base-to-emitter voltage (stepwise incident pulse).

Substituting (16) and (17) into (14) and (15), we obtain:

$$I_{E}^{n+1/2} = \alpha_{R} I_{0} \left\{ e^{\left[\frac{q}{2}(E_{z}|_{BC}^{n+1} + E_{z}|_{BC}^{n})/kT\right]} - 1 \right\}$$

$$- I_{0} \left\{ e^{-\left[\frac{q}{2}(E_{z}|_{EB}^{n+1} + E_{z}|_{EB}^{n})/kT\right]} - 1 \right\}$$

$$I_{C}^{n+1/2} = I_{0} \left\{ e^{\left[\frac{q}{2}(E_{z}|_{BC}^{n+1} + E_{z}|_{BC}^{n})/kT\right]} - 1 \right\}$$

$$- \alpha_{F} I_{0} \left\{ e^{-\left[\frac{q}{2}(E_{z}|_{EB}^{n+1} + E_{z}|_{EB}^{n})/kT\right]} - 1 \right\}.$$
(19)

Now, we obtain two coupled transcendental equations for the FD-TD electric field updates at the transistor:

$$E_{z}|_{EB}^{n+1} = E_{z}|_{EB}^{n} + \frac{\Delta t}{\epsilon_{o}} \nabla \times H|_{i,j,k}^{n+1/2} + \frac{\Delta t}{\epsilon_{o} \Delta x \Delta y} I_{E}^{n+1/2}$$

$$(20)$$

$$E_{z}|_{BC}^{n+1} = E_{z}|_{BC}^{n} + \frac{\Delta t}{\epsilon_{o}} \nabla \times H|_{i,j,k}^{n+1/2} + \frac{\Delta t}{\epsilon_{o} \Delta x \Delta y} I_{C}^{n+1/2}.$$

$$(21)$$

The Newton-Raphson method may be used to solve these equations.

To test this FD-TD modeling approach, a transistor at $T=300^\circ$ K having $I_0=10^{-16}$ amp, $\alpha_R=0.5$, and $\alpha_F=0.9901$ was modeled at the end of a 50 Ω microstrip line (of \approx 1-mil scale in the transverse plane) in the manner of Fig. 10. The collector dc supply was included in the electromagnetic simulation. Both the active ($R_c=50~\Omega$) and saturated ($R_c=10~\Omega$) regions of operation were observed for a step function excitation of the stripline. A typical result is shown in Fig. 11, where the FD-TD computed base-to-emitter voltage is compared to that obtained by a SPICE model. Very good agreement is observed.

V. CONCLUSION

Analog coupling effects for passive metallic interconnects and packaging of digital circuits operating at nanosecond clocks can be very complex. In fact, as clock speeds increase beyond 500 MHz, it may not be possible to design such systems and make them work in a timely and reliable manner without resorting to full-wave Maxwell's equations solutions

in 3-D. FD-TD numerical methods appear to provide sufficient accuracy and scaling ability for large interconnection and packaging problems to be of substantial engineering importance to the digital electronics community.

An emerging possibility is that FD-TD Maxwell's equations modeling can be linked directly to SPICE [15]. This would expand full-wave electromagnetic modeling of digital interconnects to include the voltage-current characteristics of the connected logic devices. It is conceivable that eventually the logical operation of very complex, very high-speed digital electronic circuits can be directly modeled by FD-TD time-stepping of Maxwell's equations.

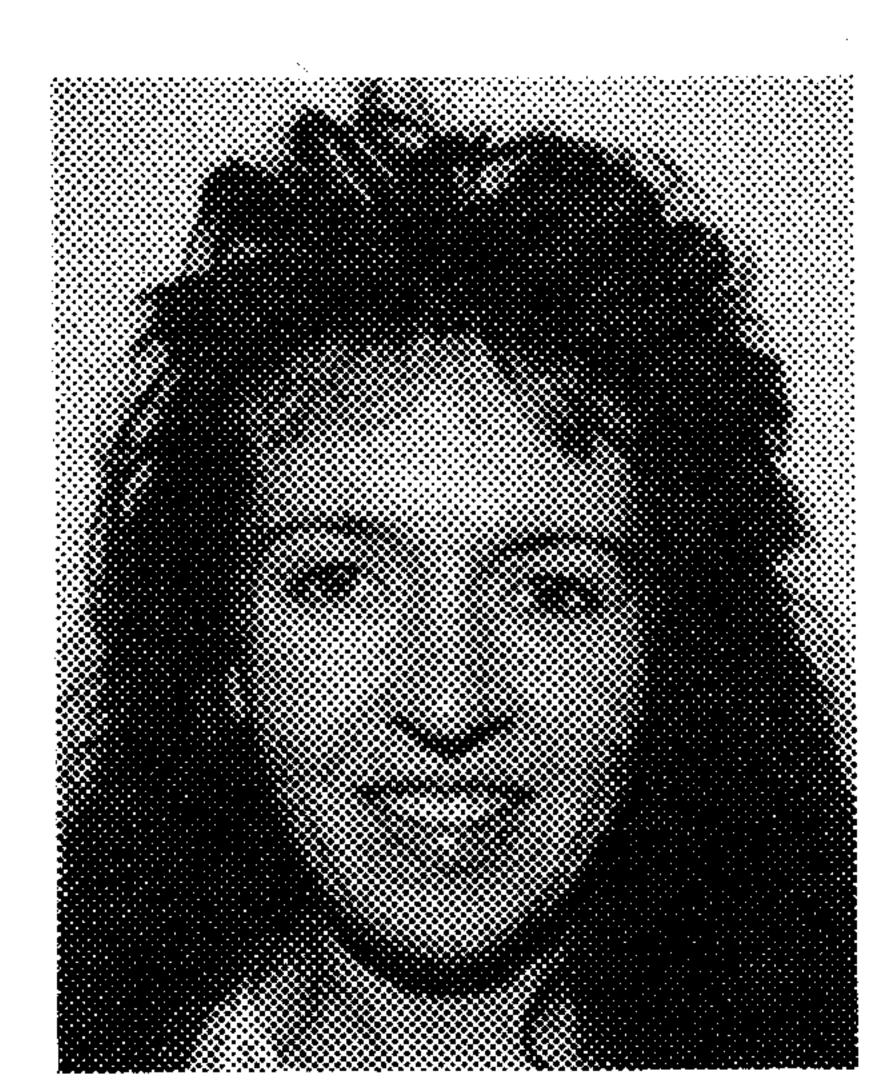
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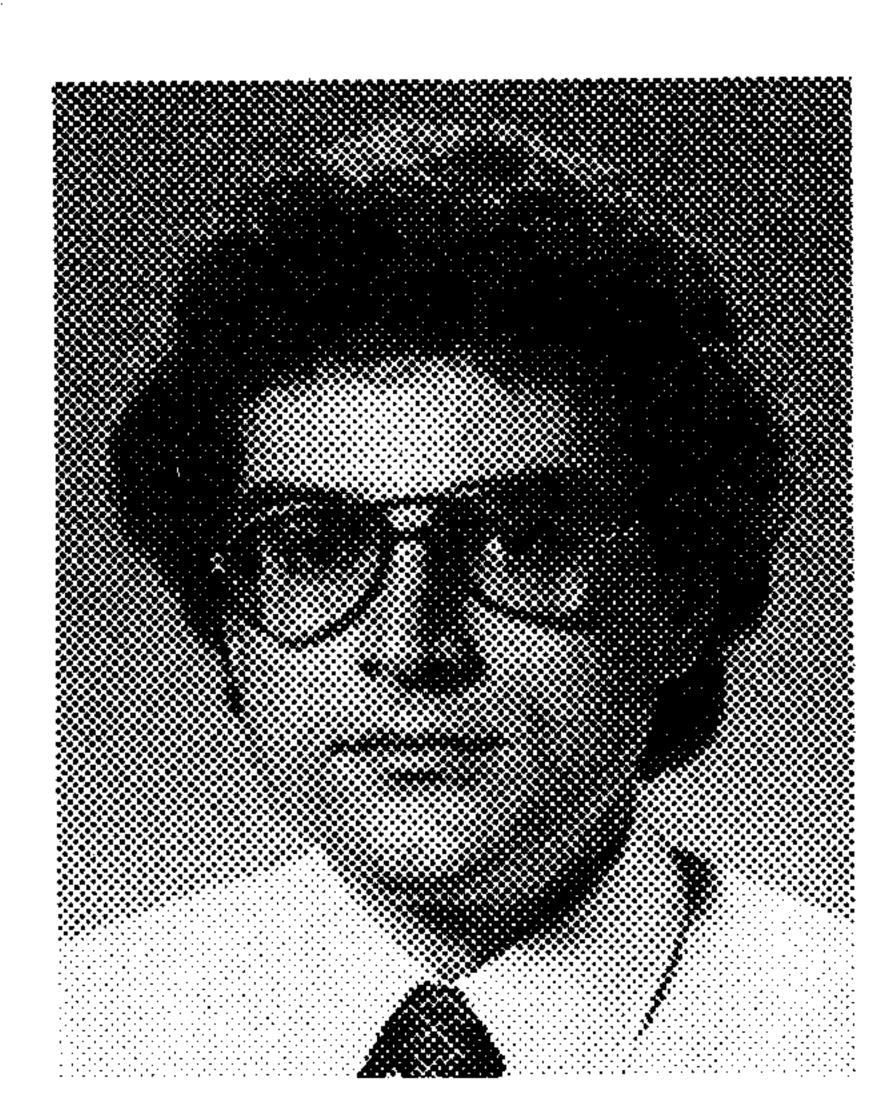
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