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EDUCATION

University of California – Los Angeles
Ph.D., Computer Science Department — *August 2003*

Northwestern University
M.S., Electrical and Computer Engineering Department — *May 2000*

Bogazici University, Istanbul, Turkey
B.S., Department of Electrical and Electronic Engineering — *July 1998*

EMPLOYMENT

Northwestern University
Professor, Dept. of Electrical Engineering and Computer Science — *September 2016*
Associate Professor, Dept. of Electrical Engineering and Computer Science — *September 2009 – August 2016*
Assistant Professor, Dept. of Electrical Engineering and Computer Science — *September2003-September2009*

Fujitsu Laboratories of America, Inc., Sunnyvale, CA
Research Intern — *June - August 2001*

University of California – Los Angeles
Research Assistant — *December 2000 – August 2003*

Northwestern University
Research Assistant — *September 1998-December 2000*

AWARDS AND HONORS

1. Best Teacher in EECS Academic Year 2012-2013.
2. Distinguished Visitor, School of Computer Science, Complutense Universidad de Madrid, March-May 2010.
3. Best Paper Award Finalist, IEEE/ACM International Conference on Computer Aided Design (ICCAD) 2007
4. National Science Foundation CAREER Award (2006)
5. Searle Center for Teaching Excellence Junior Fellow (2006-2007)
6. Best Paper Award Nomination, IEEE/ACM Design Automation Conference (DAC) 2005
7. Best Paper Award Nomination, IEEE/ACM Design Automation Conference (DAC) 2001

PUBLICATIONS

Book

Heat Management in Integrated Circuits: On-Chip and System-Level Monitoring and Cooling, S. Ogrenci-Memik, The Institution of Engineering and Technology, *2016*

Refereed Journal Publications

1. A. Del Barrio Garcia, R. Hermida, S. Ogrenci-Memik, “A Combined Arithmetic-High-Level Synthesis Solution to Deploy Partial Carry-Save Radix 8 Booth Multipliers in Datapaths”, IEEE Transactions on Computers, under review
2. D. Li, S. Joshi, J. Kim, S. Ogrenci-Memik, “End-to-end Analysis of Integration for Thermocouple-based Sensors into 3D ICs “, IEEE Transactions on VLSI, under review
3. C. Zhou, S. Chyung, J. Sun, A. Varrenti, S. Ogrenci-Memik, M. Grayson, “Thermal Sensing Using Thin-Film Thermocouples and Integrated Diagnostic Heaters”, Nanoscale and Microscale Thermophysical Engineering, under review.
4. A. Guliani, K. Zhang, S. Ogrenci-Memik, G. Memik, K. Kazutomo, R. Sankaran, P. Beckman, “Machine Learning-Based Temperature Prediction for Runtime Thermal Management across System Components”, IEEE Transactions on Parallel and Distributed Systems, under review

5. A. Del Barrio García, R. Hermida, S. Ogrenci-Memik, "A Partial Carry-Save On-the-fly Correction Multispeculative Multiplier", IEEE Transactions on Computers, Volume: 65, Issue: 11, Nov. 1 2016.
6. A. A. Del Barrio, S. Ogrenci-Memik, M. C. Molina, J. M. Mendías, R. Hermida, "Improving Circuit Performance with Multispeculative Additive Trees in High-Level Synthesis", Elsevier Microelectronics Journal 45 (2014), pp. 1470-1479.
7. B. Leung, S. Ogrenci-Memik, "Exploring Super-Resolution Implementations Across Multiple Platforms", EURASIP Journal on Advances in Signal Processing, 2013:116.
8. J. Long, D. Li, Seda Ogrenci-Memik, S. Ulgen, "Theory and Analysis for Optimization of On-Chip Thermoelectric Cooling Systems", IEEE Trans. On Computer-Aided Design of Integrated Circuits and Systems, Vol. 32, No. 10, pp. 1628-1632, 2013.
9. A. A. Del Barrio, S. Ogrenci-Memik, M. C. Molina, J. M. Mendías, R. Hermida, R., "A fragmentation aware High-Level Synthesis Flow for Low Power Heterogenous Datapaths", Integration, the VLSI Journal, Vol. 46, No. 2, pp. 119 – 130, 2013.
10. A.A. Del Barrio, R. Hermida, S. Ogrenci-Memik, J.M. Mendias M. C. Molina, "Multispeculative Addition Applied to Datapath Synthesis", IEEE Trans. On Computer-Aided Design of Integrated Circuits and Systems, Vol. 31, No. 12, pp. 1817-1830, 2012.
11. A. Varrenti, C. Zhou, A. Klock, S. Chyung, J. Long, S. Ogrenci-Memik, M. Grayson, "Thermal Sensing with Lithographically Patterned Bimetallic Thin-Film Thermocouples", IEEE Electron Device Letters, Vol. 32, No. 6, pp. 818-820, 2011.
12. A. A. Del Barrio Garcia, S. Ogrenci-Memik, M. C. Molina, J. M. Mendias, R. Hermida, "A Distributed Controller for Managing Speculative Functional Units in High Level Synthesis", IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems (TCAD), Vol. 30, No. 3, pp. 350-363, 2011
13. J. Long, J.-C. Ku, S. Ogrenci-Memik, Y. Ismail, "SACTA: A Self-Adjusting Clock Tree Architecture for Adapting to Thermal-Induced Delay Variation", IEEE Transactions on Very Large Scale Integration Systems (TVLSI), Vol. 18, No. 9, pp. 1323-1336, 2010.
14. S. Liu, S. Ogrenci-Memik, Y. Zhang, G. Memik, "An Approach for Adaptive DRAM Temperature and Power Management", IEEE Transactions on Very Large Scale Integration Systems (TVLSI), Vol. 18, No. 4, pp. 684-688, April 2010.
15. M. Ni, S. Ogrenci-Memik, "A Fast Heuristic Algorithm for Multi-Domain Clock Skew Scheduling", IEEE Transactions on Very Large Scale Integration Systems (TVLSI), Vol. 18, No. 4, pp. 630-637, April 2010.
16. A. Montone, M. D. Santambrogio, D. Sciuto, S. Ogrenci-Memik, "Placement and Floorplanning in Dynamically Reconfigurable FPGAs", ACM Transactions on Reconfigurable Technology and Systems (TRETS), Vol. 4(1), 2010.
17. F. Redaelli, M. D. Santambrogio, S. Ogrenci-Memik, "An ILP formulation for the Task Graph Scheduling Problem tailored to bi-dimensional Reconfigurable Architectures", International Journal on Reconfigurable Computing (IJRC), Vol. 2009, pp. 1-12, 2009.
18. J. Long, H. Zhou, S. Ogrenci-Memik, "EBOARST: An Efficient Edge-Based Obstacle-Avoiding Rectilinear Steiner Tree Construction Algorithm", IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems (TCAD), Vol. 27, No. 12, pp. 2169-2182, December 2008.
19. S. Ogrenci-Memik, N. Bellas, S. Mondal, "Pre-synthesis Area Estimation of Reconfigurable Streaming Accelerators", IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems (TCAD), Vol. 27, No. 11, pp. 2027-2038, November 2008.
20. R. Mukherjee, S. Liu, S. Ogrenci-Memik, S. Mondal, "A High-Level Clustering Algorithm Targeting Dual Vdd FPGAs", ACM Transactions on Design Automation of Electronic Systems (TODAES), Vol. 13, Issue 4, pp. 57-76, September 2008.
21. J. Long, S. Ogrenci-Memik, G. Memik, R. Mukherjee, "Thermal Monitoring Mechanisms for Chip Multiprocessors", ACM Transactions on Architecture and Code Optimization (TACO), Vol. 5, Issue 2, pp. 9-41, August 2008.
22. S. Ogrenci-Memik, R. Mukherjee, M. Ni, J. Long, "Optimizing Thermal Sensor Allocation for Microprocessors", IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems (TCAD), Vol. 27, No. 3, pp. 516—527, March 2008.
23. R. Mukherjee, S. Ogrenci-Memik, "An Integrated Approach to Thermal Management in High-Level Synthesis", IEEE Transactions on Very Large Scale Integration Systems (TVLSI), Vol. 14, No. 1, pp. 1165—1174, November 2006.
24. E. Kursun, R. Mukherjee, S. Ogrenci-Memik, "Early Quality Assessment for Low Power Behavioral Synthesis", Journal of Low Power Electronics (JOLPE), Vol. 1, No. 3, pp. 273—285, December 2005.
25. A. Srivastava, S. Ogrenci-Memik, B.K. Choi, M. Sarrafzadeh, "On Effective Slack Management in Post-Scheduling Phase", IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems (TCAD), Vol. 24, No. 4, April 2005.

26. S. Ogrenci-Memik, R. Kastner, E. Bozorgzadeh, M. Sarrafzadeh, “A Scheduling Algorithm for Optimization and Planning in High-level Synthesis”, ACM Transactions on Design Automation of Electronic Systems (TODAES), Vol. 10, No. 1, January 2005.
27. E. Bozorgzadeh, S. Ogrenci-Memik, X. Yang, M. Sarrafzadeh, “Routability-driven Packing: Metrics and Algorithms for Cluster-based FPGAs”, Journal of Circuits, Systems, and Computers (JCSC), Vol. 13, No. 1, February 2004.
28. S. Ogrenci-Memik, A. K. Katsaggelos, M. Sarrafzadeh, “FPGA Implementation and Analysis of an Iterative Image Restoration Algorithm”, IEEE Transactions on Computers, Vol. 52 No.3, March 2003.
29. R. Kastner, A. Kaplan, S. Ogrenci-Memik, E. Bozorgzadeh, “Instruction Generation for Hybrid Reconfigurable Systems”, ACM Transactions on Design Automation of Electronic Systems (TODAES), Vol. 7, No. 4, October 2002.
30. Ranjan, K. Bazargan, S. Ogrenci, M. Sarrafzadeh, “Fast Floorplanning for Effective Prediction and Construction”, IEEE Transactions on VLSI (TVLSI), Vol. 9, No. 2, April 2001.

Refereed Conference/Workshop Publications

1. G. Tziantzioulis, A. M. Gok, S. M. Faisal, N. Hardavellas, S. Ogrenci-Memik, S. Parthasarathy, “Lazy Pipelines: Enhancing Quality in Approximate Computing”, Design, Automation and Test in Europe (DATE), 14-18 March, 2016, Dresden, Germany
2. S M Faisal, G. Tziantzioulis, A. M. Gok, S. Parthasarathy, N. Hardavellas, S. Ogrenci-Memik, “Edge Importance Identification for Energy Efficient Graph Processing”, IEEE International Conference on Big Data, October 29-November 1, 2015, Santa Clara, CA.
3. D. Li, S. Joshi, S. Ogrenci-Memik, James Hoff, Sergo Jindariani, Tiehui Liu, Jamieson Olsen, Nhan Tran, “A Methodology for Power Characterization of Associative Memories”, IEEE International Conference on Computer Design (ICCD), October 18-21, 2015, New York, NY.
4. D. Li, G. Deptuch, J. Hoff, S. Jindariani, S. Ogrenci-Memik, T. T. Liu, J. Olsen, N. V. Tran, “Power and Thermal Characterization of the Vertically Integrated Pattern Recognition Associative Memory (VIPRAM)”, Nuclear Science Symposium, 2015, San Diego, CA
5. G. Tziantzioulis, A. M. Gok, S. M. Faisal, N. Hardavellas, S. Ogrenci-Memik, S. Parthasarathy, “b-HiVE: a bit-level history-based error model with value correlation for voltage-scaled integer and floating point units”, IEEE/ACM Design Automation Conference (DAC), 7-11 June, 2015, San Francisco, CA
6. K. Zhang, S. Ogrenci-Memik, G. Memik, K. Yoshii, R. Sankaran, P. Beckman, “Minimizing Thermal Variation Across System Components”, IEEE International Parallel & Distributed Processing Symposium, 25-28 May, 2015, Hyderabad, India
7. D. Li, S. Ogrenci-Memik, L. Henschen, “On-Chip Integration of Thermoelectric Energy Harvesting in 3D ICs”, IEEE International Conference on Circuits and Systems (ISCAS), 24-27 May, 2015, Lisbon, Portugal
8. B. Egilmez, G. Memik, S. Ogrenci-Memik, O. Ergin, “User-Specific Skin Temperature-Aware DVFS for Smartphones”, Design, Automation and Test in Europe (DATE), 14-18 March, 2015, Grenoble, France
9. D. Li, J. Kim, S. Ogrenci-Memik, “Integrating Thermocouple Sensors into 3D ICs”, International Conference on Computer Design (ICCD), October 6-9, 2013, Asheville, NC
10. A. A. Del Barrio García, R. Hermida, S. Ogrenci-Memik, “Exploring the Energy Efficiency of Multispeculative Adders”, International Conference on Computer Design (ICCD), October 6-9, 2013, Asheville, NC
11. A. A. Del Barrio Garcia, R. Hermida, S. Ogrenci-Memik, J. M. Mendías, M. C. Molina, “About the Relevance of Multispeculation in High Level Synthesis”, HLS4HPC: International Workshop on High-Level Synthesis for High-Performance Computing, January 23rd, 2012, Berlin, Germany (co-located with HiPEAC 2013)
12. A. A. Del Barrio Garcia, Román Hermida, Seda Ogrenci-Memik, José M. Mendías, María C. Molina, “Multispeculative Additive Trees in High-Level Synthesis”, Design, Automation and Test in Europe (DATE), March 18-22, 2013, Grenoble, France
13. S. Liu, S. Ogrenci-Memik, Y. Ismail, “A Comprehensive Tapered Buffer Optimization Algorithm for Unified Design Metrics”, IEEE International Symposium on Circuits and Systems (ISCAS), May 15-18, 2011, Rio de Janeiro, Brazil.
14. A. A. Del Barrio Garcia, S. Ogrenci-Memik, M. C. Molina, J. M. Mendias, R. Hermida, “'Power Optimization in Heterogenous Datapaths”, Design, Automation and Test in Europe (DATE), 14-18 March, 2011, Grenoble, France.
15. S. Liu, B. Leung, A. Neckar, S. Ogrenci-Memik, G. Memik, N. Hardavellas, “Hardware/Software Techniques for DRAM Thermal Management”, IEEE International Symposium on High-Performance Computer Architecture Conference (HPCA), February 14-16, 2011, San Antonio, TX.
16. J. Long, G. Klock, C. Zhou, S. Ogrenci-Memik, M. Grayson, “IOTA: Towards an Integrated On-chip Thermocouple Array”, International Workshop on Thermal Investigations of ICs and Systems (THERMINIC), October, 2010, Barcelona, Spain.

17. B. Leung, C. Wu, S. Ogrenci-Memik, S. Mehrotra, “An Interior Point Optimization Solver for Real Time Inter-Frame Collision Detection: Exploring Resource-Accuracy-Platform Tradeoffs”, International Conference on Field Programmable Logic and Its Applications (FPL), August 31-September 2, 2010, Milan, Italy.
18. J. Long, S. Ogrenci-Memik, “A framework for optimizing thermoelectric active cooling systems”, IEEE/ACM Design Automation Conference (DAC), July 13-18, 2010, Anaheim, CA
19. M. Ni, S. Ogrenci-Memik, “A Revisit to the Primal-Dual Based Clock Skew Scheduling Algorithm”, International Symposium on Quality Electronic Design (ISQED), March 22-24, 2010, San Jose, CA
20. A. A. Del Barrio Garcia, M. C. Molina, J. M. Mendias, R. Hermida, S. Ogrenci-Memik, “Using Speculative Functional Units in High Level Synthesis”, Design, Automation and Test in Europe (DATE), March 8-12, 2010, Dresden, Germany
21. J. Long, S. Ogrenci-Memik, M. Grayson, “Optimization of Thin-film Thermoelectric Cooler based On-chip Active Cooling System”, Design, Automation and Test in Europe (DATE), March 8-12, 2010, Dresden, Germany
22. J. Long, S. Ogrenci-Memik, “Optimization of the Bias Current Network for Accurate On-Chip Thermal Monitoring”, (Interactive Presentation) Design, Automation and Test in Europe (DATE), March 8-12, 2010, Dresden, Germany
23. J. Long, S. Ogrenci-Memik, “Inversed Temperature Dependence Aware Clock Skew Scheduling for Sequential Circuits”, (Interactive Presentation) Design, Automation and Test in Europe (DATE), March 8-12, 2010, Dresden, Germany
24. F. Redaelli, M. D. Santambrogio, V. Rana, S. Ogrenci-Memik, “Scheduling and 2D Placement Heuristics for Partially Reconfigurable Systems”, International Conference on Field-Programmable Technology (FPT), December 9-11 2009, Sydney, Australia.
25. C.-H. Wu, S. Ogrenci-Memik, S. Mehrotra, “FPGA Implementation of the Interior-Point Algorithm for Linear Programming with Applications to Collision Detection”, (Short Paper) IEEE Symposium on FPGAs for Custom Computing Machines (FCCM), April 2009, Napa, CA
26. B. Leung, Y. Pan, C. Schroeder, S. Ogrenci-Memik, G. Memik, and M. Hartmann, “Towards an "Early Neural Circuit Simulator": An FPGA Implementation of Processing In the Rat Whisker System”, International Conference on Field-Programmable Logic and Applications (FPL), September 9-11, 2008, Heidelberg, Germany
27. S. Liu, S. Ogrenci-Memik, Y. Zhang, G. Memik, “An Approach for Adaptive DRAM Temperature and Power Management”, in Proc. ACM International Conference on Supercomputing (ICS), June 7-12, 2008, Kos, Greece
28. J. Long, S. Ogrenci-Memik, “Automated Design of Self-Adjusting Pipelines”, in Proc. IEEE/ACM Design Automation Conference (DAC), June 8-13, 2008, Anaheim, CA
29. M. Ni, S. Ogrenci-Memik, “Leakage Power-Aware Clock Skew Scheduling: Converting Stolen Time into Leakage Power Reduction”, in Proc. IEEE/ACM Design Automation Conference (DAC), June 8-13 2008, Anaheim, CA
30. S. Liu, S. Ogrenci-Memik, Y. Zhang, G. Memik, “A Power and Temperature Aware DRAM Architecture”, in Proc. IEEE/ACM Design Automation Conference (DAC), June 8-13 2008, Anaheim, CA
31. J. Long, H. Zhou, S. Ogrenci-Memik, “An O(nlogn) Edge-Based Algorithm for Obstacle-Avoiding Rectilinear Steiner Tree Construction”, in Proc. ACM International Symposium on Physical Design (ISPD), April 13-16, 2008, Portland, OR
32. M. Santambrogio, M. Gianni, S. Ogrenci-Memik, “Managing Reconfigurable Resources in Heterogeneous Cores using Portable Pre-Synthesized Templates”, in Proc. International Symposium on System-on-Chip, November 19-21, 2007, Tampere, Finland
33. M. Ni, S. Ogrenci-Memik, “Early Planning for Clock Skew Scheduling during Register Binding”, in Proc. IEEE/ACM International Conference on Computer Aided Design (ICCAD), November 5-8, 2007, San Jose, CA
34. J. Long, J. Ku, S. Ogrenci-Memik, Y. Ismail, “A Self-Adjusting Clock Tree Architecture to Cope with Temperature Variations”, in Proc. IEEE/ACM International Conference on Computer Aided Design (ICCAD), November 5-8, 2007, San Jose, CA **[IEEE/ACM William J. McCalla ICCAD Best Paper Award Finalist]**
35. M. Santambrogio, V. Rana, S. Ogrenci-Memik, U. Acar, D. Scuito, “A Novel SoC Design Methodology Combining Adaptive Software and Reconfigurable Hardware”, in Proc. IEEE/ACM International Conference on Computer Aided Design (ICCAD), November 5-8, 2007, San Jose, CA
36. M. Ni, S. Ogrenci-Memik, “Self-Heating-Aware Optimal Wire-Sizing Under Elmore Delay Model”, in Proc. Design, Automation and Test in Europe (DATE), 16-20 April, 2007, Niece, France
37. Marco Santambrogio, Vincenzo Rana, Seda Ogrenci-Memik and Donatella Sciuto, “Combining Hardware Reconfiguration and Adaptive Computation for a Novel SoC Design Methodology”, in Proc. IEEE International Conference on Field-Programmable Technology (FPT), December 13-15, Bangkok, Thailand
38. R. Mukherjee, S. Mondal, S. Ogrenci-Memik, “Thermal Sensor Allocation and Placement for Reconfigurable Systems”, in Proc. IEEE/ACM International Conference on Computer-Aided Design (ICCAD), November 5-9 2006, San Jose, CA

39. R. Mukherjee, S. Ogrenci-Memik, “Physical Aware Frequency Selection for Dynamic Thermal Management in Multi-Core Systems”, in Proc. IEEE/ACM International Conference on Computer-Aided Design (ICCAD), November 5-9 2006, San Jose, CA
40. M. Ni, S. Ogrenci-Memik, “Thermal-Induced Leakage Power Optimization by Redundant Resource Allocation”, in Proc. IEEE/ACM International Conference on Computer-Aided Design (ICCAD), November 5-9 2006, San Jose, CA
41. S. Ogrenci-Memik, M. Santambrogio, G. Agosta, “Adaptive Metrics for System-Level Functional Partitioning”, in Proc. Forum on Specification and Design Languages (FDL), September 19-22 2006, Darmstadt, Germany
42. S. Mondal, S. Ogrenci-Memik, N. Bellas, “Pre-Synthesis Area Estimation of Reconfigurable Streaming Accelerators”, in Proc. International Conference on Field Programmable Logic and Applications (FPL), August 28-30 2006, Madrid, Spain
43. R. Mukherjee, S. Ogrenci-Memik, “Systematic Temperature Sensor Allocation and Placement for Microprocessors”, in Proc. IEEE/ACM Design Automation Conference (DAC), July 24-28, 2006, San Francisco, CA
44. R. Mukherjee, S. Mondal, S. Ogrenci-Memik, “A Sensor Distribution Algorithm for FPGAs with Minimal Dynamic Reconfiguration Overhead”, in Proc. International Conference on Engineering of Reconfigurable Systems and Algorithms (ERSA), June 26-29, 2006, Las Vegas, NV
45. S. Mondal, R. Mukherjee, S. Ogrenci-Memik, “Fine-Grain Thermal Profiling and Sensor Insertion for FPGAs”, in Proc. IEEE International Symposium on Circuits and Systems (ISCAS), May 21-24 2006, Kos, Greece
46. S. Mondal, S. Ogrenci-Memik, N. Bellas, “Pre-synthesis Queue Size Estimation of Streaming Data Flow Graphs (Poster Presentation, 2-page extended abstract in the proceedings), IEEE Symposium on FPGAs for Custom Computing Machines (FCCM), April24-26, 2006, Napa, CA
47. D. Nguyen, G. Memik, S. Ogrenci-Memik, and A. Choudhary, “Real-Time Feature Extraction for High Speed Networks”, in Proc. International Conference on Field Programmable Logic and Applications (FPL), August 24-26 2005, Tampere, Finland
48. R. Mukherjee, S. Ogrenci-Memik, G. Memik, “Peak Temperature Control and Leakage Reduction During Binding in High-Level Synthesis”, in Proc. ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED), August 8-10 2005, San Diego, CA
49. R. Mukherjee, S. Ogrenci-Memik, G. Memik, “Temperature-aware Resource Allocation and Binding in High-Level Synthesis”, in Proc. IEEE/ACM Design Automation Conference (DAC), June 13-17 2005, Anaheim, CA **[Best Paper Award Nomination]**
50. S. Mondal, S. Ogrenci-Memik, “A Low Power FPGA Routing Architecture”, in Proc. IEEE International Symposium on Circuits and Systems (ISCAS), May 23-26 2005, Kobe, Japan.
51. S. Mondal, S. Ogrenci-Memik, “Fine-Grain Leakage Optimization in SRAM based FPGAs”, in Proc. Great Lakes Symposium on VLSI (GLSVLSI), April 17-19, Chicago, IL
52. R. Jafari, S. Ogrenci-Memik, M. Sarrafzadeh, “Quick Reconfiguration in Clustered Micro-Sequencer”, International Parallel and Distributed Processing Symposium (IPDPS), in Proc. Reconfigurable Architectures Workshop (RAW), April 4-5 2005, Denver, CO
53. S. Mondal, S. Ogrenci-Memik, D. Das, “Hierarchical LUT Structures for Leakage Power Reduction” Poster Presentation, ACM International Symposium on Field Programmable Gate Arrays (FPGA), February 20-22 2005, Monterey, CA
54. S. Mondal, S. Ogrenci-Memik, “Resource Sharing in Pipelined CDFG Synthesis”, in Proc. IEEE/ACM Asia-South Pacific Design Automation Conference (ASP-DAC), January 18-21, Shanghai, China
55. R. Mukherjee, S. Ogrenci-Memik, “Evaluation of Dual Vdd Fabrics for Low Power FPGAs”, in Proc. IEEE/ACM Asia-South Pacific Design Automation Conference (ASP-DAC), January 18-21, Shanghai, China
56. R. Mukherjee, S. Ogrenci-Memik, “Power-driven Design Partitioning”, in Proc. International Conference on Field-Programmable Logic and Its Applications (FPL), August 30 –September1 2004, Antwerp, Belgium
57. R. Mukherjee, S. Ogrenci-Memik, “Power Management for FPGAs: Power-driven Design Partitioning” (Poster Presentation, 2-page extended abstract included in the proceedings), IEEE Symposium on FPGAs for Custom Computing Machines (FCCM), April 2004, Napa, CA
58. A. Srivastava, S. Ogrenci-Memik, B. K. Choi, M. Sarrafzadeh, “Achieving Design Closure through Delay Relaxation Parameter ”, in Proc. IEEE/ACM International Conference on Computer-Aided Design (ICCAD), November 2003, San Jose, CA
59. S. Ogrenci-Memik, G. Memik, R. Jafari, E. Kursun, “Global Resource Sharing for Synthesis of Control Data Flow Graphs on FPGAs”, in Proc. IEEE/ACM Design Automation Conference (DAC), June 2003, Anaheim, CA
60. S. Ogrenci-Memik, F. Fallah, “Accelerated SAT-based Scheduling of Control/Data Flow Graphs”, in Proc. International Conference on Computer Design (ICCD), September 2002, Freiburg, Germany

61. E. Kursun, A. Srivastava, S. Ogrenci-Memik, M. Sarrafzadeh, "Early Evaluation Techniques for Low Power Binding", in Proc. ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED), August 2002, Monterey, CA
62. E. Bozorgzadeh, S. Ogrenci-Memik, R. Kastner, M. Sarrafzadeh, "Pattern Selection: Customized Block Allocation for Domain-Specific Programmable Systems", in Proc. International Conference on Engineering of Reconfigurable Systems and Algorithms (ERSA), June 2002, Las Vegas, NV
63. S. Ogrenci-Memik, F. Fallah, "Accelerated Boolean Satisfiability-Based Scheduling for High-Level Synthesis", IEEE/ACM International Workshop on Logic & Synthesis (IWLS), June 2002, New Orleans, LA.
64. G. Memik, S. Ogrenci-Memik, W. H. Mangione-Smith, "Design and Analysis of a Layer Seven Network Processor Accelerator Using Reconfigurable Logic", in Proc. IEEE Symposium on FPGAs for Custom Computing Machines (FCCM), April 2002, Napa, CA.
65. E. Bozorgzadeh, R. Kastner, S. Ogrenci-Memik and M. Sarrafzadeh, "Pattern Selection in Programmable Systems" (poster presentation), ACM International Symposium on Field Programmable Gate Arrays (FPGA), February 2002, Monterey, CA.
66. S. Ogrenci-Memik, E. Bozorgzadeh, R. Kastner, M. Sarrafzadeh, "A Super-Scheduler for Embedded Reconfigurable Systems", in Proc. IEEE/ACM International Conference on Computer Aided Design (ICCAD), November 2001, San Jose, CA
67. R. Kastner, S. Ogrenci-Memik, E. Bozorgzadeh, M. Sarrafzadeh, "Instruction Generation for Hybrid Reconfigurable Systems", in Proc. IEEE/ACM International Conference on Computer Aided Design (ICCAD), November 2001, San Jose, CA
68. K. Bazargan, S. Ogrenci, M. Sarrafzadeh, "Integrating Scheduling and Physical Design into a Coherent Compilation Cycle for Reconfigurable Computing Architectures", in Proc. IEEE/ACM Design Automation Conference (DAC), June 2001, Las Vegas, NV [Best Paper Award Nomination]
69. S. Ogrenci-Memik, E. Bozorgzadeh, R. Kastner, M. Sarrafzadeh, "SPS: A Strategically Programmable System", International Parallel and Distributed Processing Symposium (IPDPS), Reconfigurable Architectures Workshop (RAW), April 2001, San Francisco, CA
70. E. Bozorgzadeh, S. Ogrenci-Memik, M. Sarrafzadeh, "RPack: Routability-Driven Packing for Cluster-Based FPGAs", in Proc. Asia-South Pacific Design Automation Conference (ASP-DAC), January 2001, Yokohama, Japan
71. S. Ogrenci, K. Bazargan, M. Sarrafzadeh, "Image Analysis and Partitioning for FPGA Mapping", in Proc. IEEE Workshop on Signal Processing Systems (SiPS), October 2000, Lafayette, LA
72. K. Bazargan, R. Kastner, S. Ogrenci, M. Sarrafzadeh, "A C to Hardware/Software Compiler", (Poster Presentation, 2-page extended abstract included in the proceedings), IEEE Symposium on FPGAs for Custom Computing Machines (FCCM), April 2000, Napa Valley, CA
73. S. Ogrenci, A. K. Katsaggelos, M. Sarrafzadeh, "FPGA Implementation and Analysis of Image Restoration" (poster presentation), ACM International Symposium on Field Programmable Gate Arrays (FPGA), February 2000, Monterey, CA

Book Chapters

74. E. Bozorgzadeh, R. Kastner, S. Ogrenci-Memik, M. Sarrafzadeh, "Strategically Programmable Systems", The Computer Engineering Handbook, CRC Press, December 2001
75. E. Bozorgzadeh, A. Kaplan, R. Kastner, S. Ogrenci-Memik, M. Sarrafzadeh, "Optimization for Reconfigurable Systems Using Hierarchical Abstraction", J. Cong and J. R. Shinnerl (editors), Multilevel Optimization and VLSICAD, Kluwer Academic Publishers, Boston, 2002

Patents

1. System and Method for Tracking Content in a Medicine Container, *Provisional Application Submitted, January 21, 2015*, Serial No. 62/105,966, Sanjay Mehrotra, Seda Ogrenci-Memik, Ilya Mikhelson
2. Bimetallic Integrated On-Chip Thermocouple Array, U.S. Patent Number: 8,517,605, August 27, 2013, NU Reference Number: NU2009-146-02 (29146), Inventors: Matthew A. Grayson, Seda Memik, Jieyi Long, Chuanle Zhou, Andrea Grace Klock

PROFESSIONAL ACTIVITIES

- Editorial Boards
  - IEEE Transactions on Very Large Scale Integration Systems (TVLSI), Associate Editor, Jan. 2007-2013
  - International Journal on Reconfigurable Computing, April 2011-present
- Organizer, Workshop on FPGAs for Scientific Simulation and Data Analytics, (co-organized with Argonne Labs and National Center for Supercomputing Applications), October 12-14, 2016, Urbana, IL
- Program Co-Chair, International Conference on Embedded and Ubiquitous Computing (EUC)- 2015
- Visiting Scholar, Argonne National Labs, Spring Quarter 2014 (Northwestern Argonne Institute of Science and Engineering, Mini-Sabbatical Program)
- Conference Organizing Committee
  - Publication Chair, International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), 2015
  - Poster Chair, 21st Reconfigurable Architectures Workshop (RAW) 2013
  - Publicity Co-Chair, International Symposium on Field Programmable Logic and Its Applications (FPL) 2010
  - Local Arrangements Co-Chair for the Great Lakes Symposium on VLSI (GLSVLSI) 2005
- Leadership in Technical Program Committees (TPCs)
  - *Design Automation Track Chair*, Embedded and Ubiquitous Computing Conference (EUC), 2013, 2014
  - *Design Automation Track Chair*, Asia South Pacific Quality Electronic Design (ASQED) 2010, 2011, 2012
  - *VLSI-CAD Track Co-Chair*, International Symposium on VLSI (ISVLSI) 2009
  - *System Design Track Chair*; IEEE/ACM International Conference on Computer Aided Design (ICCAD) (2007)
  - *High-Level Synthesis Track Chair*; IEEE/ACM International Conference on Computer Aided Design (ICCAD) (2006)
- TPC Membership
  - IEEE/ACM Design Automation Conference (DAC) 2013, 2014, 2015
  - IEEE/ACM International Conference on Computer Aided Design (ICCAD) 2004-2007, 2011-2013
  - Design, Automation and Test in Europe (DATE) 2006, 2015, 2016
  - International Conference on High Performance and Embedded Architectures and Compilers (HiPEAC) 2011
  - International Symposium on Field Programmable Logic and Its Applications (FPL) 2005-2016
  - Reconfigurable Architectures Workshop (RAW) 2008-2016
  - Great Lakes Symposium on VLSI (GLSVLSI) 2004-2009
  - Applied Reconfigurable Computing (ARC) Workshop (ARC) 2007-2016
  - Southern Conference on Programmable Logic (SPL) 2008-2012
  - International Conference on ReConFigurable Computing and FPGAs (ReConFig) 2014-2016
  - International Workshop on Reconfigurable Communication-centric Systems-on-Chip, 2013, 2014
- Chaired sessions at ICCAD, FPL, ISCAS.
- Served on NSF Panels between 2003-present
- Reviewer for over 30 conferences and journals, i.e., every major conference and journal in CAD, Reconfigurable Computing, Computer Architecture, and VLSI.

Invited Talks

1. "High Level Synthesis Flows for Reconfigurable Systems", Argonne National Labs, January 21, 2016.
2. "Thermal Aware Design and Management of Main Memory Systems", Northwestern-Tel Aviv University Workshop, February 23, 2015, Tel-Aviv, Israel.
3. "The Need for Thermal-Aware Run-time Systems", All Hands Workshop-ARGO Project, Argonne National Labs, July 29, 2014.
4. "Thermal Aware Design for Main Memory Systems", Argonne National Labs, September 19, 2013.
5. "Thermal Aware Design and Optimizations for High Performance Integrated Circuits", Electrical and Computer Engineering Department, Illinois Institute of Technology, September 16, 2011.
6. "Thermal Aware Design and Optimizations for High Performance Integrated Circuits", Electrical and Computer Engineering Department, University of Wisconsin-Madison, February 11, 2011.

7. “Thermal Issues in High Performance Integrated Circuits”, Electrical Engineering Department, Politecnico di Milano, Milan, Italy, May 20, 2010.
8. “Tools for Optimization of Active Cooling Systems for MPSoCs”, Workshop on Compiler Assisted System-on-Chip Assembly, Grenoble, France, October 11, 2009.
9. “Design Automation for Thermal Effects and Other Sources of Variation: An Overview”, School of Engineering and Sciences, Sabanci University, Istanbul, Turkey, September 9, 2009.
10. “Thermal-Aware Design”, Integrated Systems Center, École Polytechnique Fédérale de Lausanne (EPFL), Lausanne, Switzerland, September 10, 2008.
11. “Design and Optimization of Thermal Monitoring Infrastructures”, IMEC, Leuven, Belgium, September 5, 2008.
12. “Thermal-Aware Design”, Electrical and Computer Engineering Department, University of Wisconsin-Madison, February 29, 2008
13. “Thermal-Aware Synthesis”, Strategic CAD Labs, Intel Inc, November 20, 2005, Hillsboro, OR
14. “An Architecture Exploration and Synthesis Framework for Reconfigurable Fabrics”, Center for Embedded Hardware Systems Research, Motorola Inc., February 15, 2005, Schaumburg, IL.
15. “Overview of Embedded and Hybrid Systems Research”, Privacy and Security Technologies Lab, Motorola Inc., July 28, 2004, Schaumburg, IL
16. “CAD Tools and Architectures for Low Power FPGAs”, Xilinx Inc., February 20, 2004, San Jose, CA

ADVISING, TEACHING, AND UNIVERSITY SERVICE

Current Graduate Students

Yingyi Luo, PhD student (Fall 2015)

Siddhartha Joshi, PhD student (Fall 2014)

Dawei Li, PhD student (Fall 2011)

Kaicheng Zhang (co-Advisor: Gokhan Memik), PhD student (Fall 2011)

Alumni

- PhD

  - Brian Leung, August 2012. Thesis: Performance and Energy Optimizations for DRAM Memory Systems. Current Position: Intel, Inc., Xeon Phi Architect.

  - Song Liu, August 2011. Thesis: Architectural and OS-Level Performance and Thermal Optimizations for DRAM Systems. Current Position: Facebook, Inc.

  - Jieyi Long, March 2010. Thesis: Design of Thermal Monitoring Infrastructures and Thermal Optimizations for High Performance Chips. Current Position: Magma Design Automation.

  - Min Ni, March 2009. Thesis: Thermal Aware and Low Power Optimizations for VLSI Synthesis. Current Position: Synopsys, Inc.

  - Somsubhra Mondal, June 2007. Thesis: Architectural Optimizations and Synthesis Tools for Improved Energy Efficiency and Faster Design Closure for FPGAs. Current position: Ronin Capital

  - Rajarshi Mukherjee, June 2006. Thesis: Thermal-aware design and analysis techniques for integrated circuits and high-performance microprocessor systems. Current position: Apple, Inc.

- MS

  - Yifan Guo 2016 (Thesis), Ryan Cortez 2010 (Project), Chih-Hung Wu 2009 (Thesis)

  - Academic Advisor for four to five course-based terminal MS students each year

Thesis Defense Committees

- PhD Thesis Committee

  Giorgios Tziantoulis, Yuankai Chen, Li Li, Chuanle Zhou, Pablo Ituero (external member, Universidad Politecnica de Madrid) Alberto del Barrio Garcia (external member, Complutense Universidad de Madrid), Brian Leung (chair), Song Liu (chair), Jieyi Long (chair), Min Ni (chair), Somshubra Mondal (chair), Rajarshi Mukherjee (chair), Yan Pan, Alex Shye, Me Keng, Ruiming Chen, Zhenyu Gu, Ja Chun Ku, DiaaEldin Khalil, Nikos Liveris, Serkan Ozdemir, Ahmed Shebaita, Jia Wang, Joseph Zambreno, David Zaretsky

- MS Thesis Committee

  Ke Liu, Seung Chyung, Emre Karaman, Utku Pamuksuz, Ryan Cortez (chair), Chih-Hung Wu (chair), Anitha Mohan, David Nguyen, Seunghoon Kim, Sanghamitra Roy

University/Department Committees

- Office for Research Limited Submissions Advisory Committee, 2016-present
- Class Coordinator, McCormick Murphy Scholars Program (2015-present)
- Member, Northwestern Undergraduate Research (URG) Committee (2014-present)
- Computer Engineering Chair for EECS Graduate Admissions (2014-present)
- Chair, Computer Engineering Faculty Search Committee (2013-2014 Academic Year)
- Co-Chair, Computer Engineering Graduate Committee (2013-2014)
- Chair, Publicity, Alumni, and Industrial Relations Committee (2011 – present)
- Member, Computer Engineering Undergraduate Curriculum Committee (2003-present)
- Member, EECS Diversity Committee (2013-present)
- Member, Undergraduate Recruiting Committee (2006-present)
- Academic Advisor to the Women In Computing, student group (2010-2014)
- Member, Database Systems Faculty Search Committee (2013-2014 Academic Year)
- Co-Chair, VLSI Faculty Search Committee (2012-2013 Academic Year)
- Chair, Computer Engineering Undergraduate Curriculum Committee (2008-2010)
- Member, McCormick School of Engineering Curriculum Committee (2009-2010)
- Member, Computer Science Undergraduate Curriculum Committee (2006-2007 Academic year)