Northwestern University
Electrical Engineering and Computer Science
EECS357: Introduction to VLSI CAD
Prof. Hai Zhou

Feb 4, 2014
Handout #5
Due: Feb 11

Homework 3

You may discuss the assignments with your classmates but need to write down your solutions independently. Be careful with your handwriting. Unclear solutions will be assumed to be wrong.

1. (20 points) Exercise 3.10 on page 155.
2. (20 points) Exercise 3.17 on page 157.
3. (20 points) Prove that the sum of the cutsizes over all $r-1$ horizontal and $s-1$ vertical cutlines across an $r \times s$ gate-array master is the same as the total wire length according to the half-perimeter estimate.
4. (40 points) Programming assignment: implement an algorithm for linear placement, that is, to place the cells in one row. The input is a netlist that gives the number of cells and the connection between the cells. Assume each cell has a unit width, thus can be placed on the integer positions. You may select your approach from similated annealing, partitioning based, iterative construction, or any other approaches. We will select as the champion a program that gives the minimal wire length for a set of inputs, and give it a bonus credit of 30 points. To make the competition easy, please use the following format for input:

   number_of_cells number_of_nets
   cell1 cell2 cell3 cell4 /* a net connecting 4 cells */
   cell1 cell2 /* another net */
   ...